Article

Selenium-alloyed tellurium oxide for amorphous p-channel transistors

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Compared to polycrystalline semiconductors, amorphous semiconductors offer inherent cost-effective, simple and uniform manufacturing. Traditional amorphous hydrogenated Si falls short in electrical properties, necessitating the exploration of new materials. The creation of high-mobility amorphous n-type metal oxides, such as a-InGaZnO (ref. 1), and their integration into thin-film transistors (TFTs) have propelled advancements in modern large-area electronics and new-generation displays[2–8]. However, finding comparable p-type counterparts poses notable challenges, impeding the progress of complementary metal–oxide–semiconductor technology and integrated circuits[9–11]. Here we introduce a pioneering design strategy for amorphous p-type semiconductors, incorporating high-mobility tellurium within an amorphous tellurium suboxide matrix, and demonstrate its use in high-performance, stable p-channel TFTs and complementary circuits. Theoretical analysis unveils a delocalized valence band from tellurium $5p$ bands with shallow acceptor states, enabling excess hole doping and transport. Selenium alloying suppresses hole concentrations and facilitates the p-orbital connectivity, realizing high-performance p-channel TFTs with an average field-effect hole mobility of around 15 $cm^2 V^{-1} s^{-1}$ and on/off current ratios of 10^6–10^7, along with wafer-scale uniformity and long-term stabilities under bias stress and ambient ageing. This study represents a crucial stride towards establishing commercially viable amorphous p-channel TFT technology and complementary electronics in a low-cost and industry-compatible manner.

Creating high-mobility amorphous p-type oxide semiconductors holds the promise of enhancing scalable complementary metal–oxide–semiconductor (CMOS) technology and facilitating the integration of multifunctional electronics. However, the current hurdle lies in the highly localized valence band maximum (VBM) states, consisting of anisotropic oxygen $2p$ orbitals. In conventional p-type oxides such as Cu_2O and SnO, the valence band orbital hybridization imparts decent p-type characters whereas the device performance remains constrained, even with the crystalline channel[11–15]. Whereas using amorphous hydrogenated Si for cost-effective, large-area production is a viable option, its low field-effect hole mobility ($\mu_h < 0.1$ $cm^2 V^{-1} s^{-1}$) restricts its modern applications. Benefiting from the high mobility and stability, low-temperature polycrystalline silicon is combined at present with n-type oxides for complementary circuit and display backplane applications. Nevertheless, this use is confined to small- and/or medium-area devices due to the intricate process flow, inhomogeneity from the grain boundary and challenges in upscaling mass production[16]. Extensive efforts have been directed towards exploring organic compounds[17,18], metal halides[19–22] and low-dimensional nanomaterials[23–29] as p-type semiconductors for transistors. However, these materials show optimal performance only in crystallized form and they come with intrinsic limitations such as low stability, complex synthesis processes, large-area non-uniformity and a lack of industrial compatibility.

In this study, we propose an alternative route to designing amorphous p-type semiconductor, which involves a mixed phase of high-mobility tellurium within an amorphous tellurium suboxide matrix (Te–TeO_x, $0 < x \leq 2$). The thermal evaporation method was used to deposit amorphous Te–TeO_x thin films by evaporating tellurium dioxide (TeO_2) powder, followed by low-temperature annealing under ambient conditions at 225 °C. For the deposition of Se-alloyed Te–TeO_x, Se was blended with TeO_2 powder before the evaporation (more details in the Methods). The Se addition had no impact on the microstructure, nevertheless, it was instrumental in improving the electrical properties (which we discuss later). The X-ray diffraction (XRD) patterns show the typical amorphous features of deposited films before and after thermal annealing (Fig. 1a). High-resolution transmission electron microscopy (HRTEM) and diffraction analyses confirmed the amorphous-like nature, showing no perceptible crystalline domains or long-range orders (Fig. 1b,c). This amorphous and short-range disorder microstructure aligns with previous observations on evaporated tellurium oxide[30–32].

The Te K-edge X-ray absorption near edge structure (XANES) spectrum of the deposited film shows characteristics resembling a mixture

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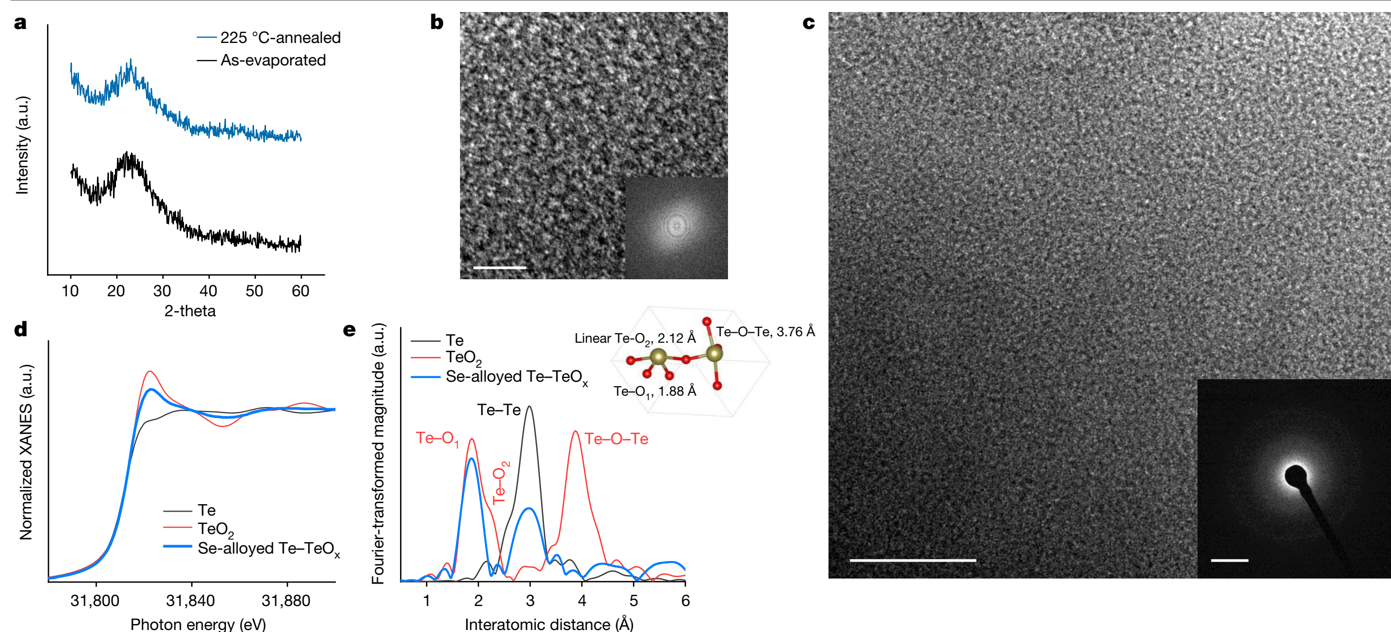

Fig. 1 | Structural characterizations of amorphous Se-alloyed Te–TeO$_x$. **a**, XRD spectra of as-evaporated and 225 °C-annealed Se-alloyed Te–TeO$_x$ thin films on glass. **b**,**c**, HRTEM images, the fast Fourier transform spot patterns (**b**, inset) and selected area electron diffraction pattern of 225 °C-annealed Se-alloyed Te–TeO$_x$ (**c**, inset). **d**, Te K-edge XANES spectra of the Se-alloyed Te–TeO$_x$ film and reference materials of elemental Te and TeO$_2$. **e**, Corresponding Fourier transform of Te K-edge k^3-weighted EXAFS spectra. The inset shows the tetragonal TeO$_2$ bonding model. Scale bars, 5 nm (**b**), 20 nm (**c**) and 51/nm (**c**, inset). a.u., arbitrary units.

of Te and TeO$_2$ reference spectral features (Fig. 1d). A linear combination analysis indicates an averaged Te/TeO$_2$ composition ratio of roughly 4/6 (detailed discussion in Supplementary Methods), and the atomic ratio of Te/O was estimated to be 1/1.2. Compared to reference TeO$_2$ with peak feature of shorter Te–O$_1$ and longer Te–O$_2$, the Fourier transform for extended X-ray absorption fine structure (EXAFS) of the deposited film clearly shows a slight decrease in the shorter Te–O$_1$ bond and the sharp diminishing of both longer Te–O$_2$ and Te–O–Te long-range ordering (Fig. 1e and Extended Data Fig. 1). The generation of oxygen vacancy breaks the bridged bond of Te–O$_2$, and the undercoordinated Te leads to the loss of Te–O–Te long-range ordering, forming the amorphous structure. Furthermore, noticeable metallic Te–Te bonds were observed, suggesting the spontaneous generation of elemental Te in the final films. The several components were further confirmed by X-ray photoelectron spectroscopy analysis (Extended Data Fig. 2). This can be related to the redox behaviour of tellurium, in which partial Te^{4+} was reduced to elemental Te in molten TeO$_2$ in an inert atmosphere[32] and with the tungsten boat reaction[33]. Therefore, it is plausible that the composite film is composed of a mixed phase of Te–TeO$_x$.

As elemental Te is present, the likelihood of local Te nanocrystals cannot be ruled out. However, their embeddedness and dispersion within the amorphous TeO$_x$ matrix tend to induce short-range disordering. Furthermore, using an amorphous substrate at room temperature is beneficial to the formation of a highly disordered amorphous-like structure. The heavy dissociation of TeO$_2$ during evaporation could lead to the simultaneous impingement of Te and TeO$_x$ on the substrate and the limited mobility and mutual solubility of the adsorbed atoms on the substrate can result in condensation at or near the impingement point before reaching a more energetically favourable site.

Leveraging the insights gained from XANES and EXAFS results and the film density of 5.6 g per cm^3 obtained from X-ray reflectivity analysis, we conducted density functional theory (DFT) calculations to explore the energy band structure and electrical properties of amorphous Te–TeO$_x$. For stoichiometric amorphous TeO$_2$, the VBM primarily consists of localized O-2p states, indicating the poor p-type character (Extended Data Fig. 3). This stands in marked contrast to recent studies on orthorhombic low-dimensional β-TeO$_2$, which shows favourable p-type properties[34–36]. For non-stoichiometric amorphous Te–TeO$_x$, the radial distribution functions (RDFs) generated in DFT indicate the diminishment of long Te–O$_2$ bond (Fig. 2a). The generated atomic structure in Fig. 2b encompasses a variety of Te–Te bonds and undercoordinated (zero-, one-, two- and threefold) Te atoms with oxygen. The average coordination number of Te with oxygen is calculated to be 2.5. The electronic density of states illustrates that the VBM is dominated by partially occupied Te-5p defect bands above the O-2p states (Fig. 2c). The Te-5p states, originating mainly from Te in Te–TeO$_x$, serve as the hole transport channel and act as shallow acceptors. The spatially dispersed and percolated Te-5p orbitals throughout the amorphous network, along with enough Te in Te–TeO$_x$, contribute to the dispersed VBM. The charge densities of the Te-5p defect band and the shallow acceptor state near Te-5p defect band are illustrated in Fig. 2d,e, respectively. The theoretical bandgap of TeO$_{1.2}$ is 0.91 eV in HSE06 (0.49 eV in DFT-PBE (Perdew–Burke–Ernzerhof)), slightly lower than the experimental value of around 1.1 eV (Extended Data Fig. 4).

To assess the potential of Te–TeO$_x$-based semiconductors for electronic device applications, we fabricated bottom-gate, top-contact TFTs by depositing films on a 100 nm SiO$_2$ dielectric containing Ni source and drain electrodes. The transfer and output characteristics are presented in Fig. 3a,b. The pristine Te–TeO$_x$ TFT showed typical p-channel behaviour with an average μ_h of 4.2 cm^2 V^{-1} s^{-1} and an on/off current ratio (I_{on}/I_{off}) of around 10^4. The onset voltage showed a pronounced positive shift, indicating a relatively high hole concentration in the channel. The TFT performance notably improved with Se doping, evident from a reduced onset voltage, lowered off-state current and increased μ_h. The optimized Se alloying atomic percentage was determined to be around 25% (Se/Te, 1/3) using high-resolution inductively coupled plasma mass spectrometry (Extended Data Fig. 5). The deposited Se-alloyed Te–TeO$_x$ TFTs delivered an average μ_h of around 15 cm^2 V^{-1} s^{-1} (forward scan; μ_h from reverse scan is around 14 cm^2 V^{-1} s^{-1}), an I_{on}/I_{off} of roughly 10^7 and onset voltages of 20–25 V, whereas higher Se alloying percentages were found to degrade the TFT performance with a notable n-doping effect. Similar to many semiconductors, the

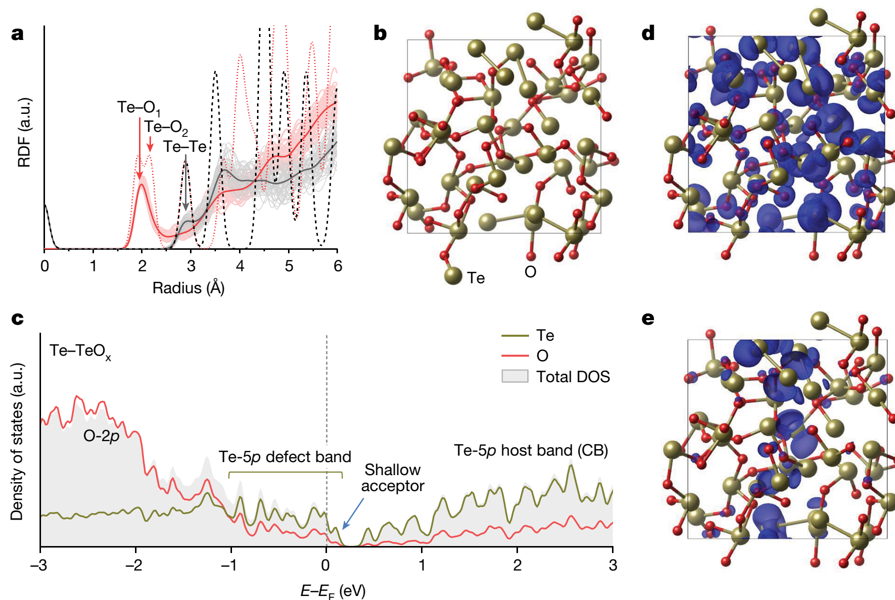

Fig. 2 | Atomic and electronic structures. a, Averaged Te–O (red) and Te–Te (black) RDFs of amorphous Te–TeO_x (Te/O atomic ratio 1/1.2) generated in DFT. Light red and grey lines are the Te–O and Te–Te RDFs for all the 50 generated Te–TeO_x samples; those for the crystalline TeO_2 and Te are shown with dashed lines. **b**, Atomic structure of amorphous Te–TeO_x generated in DFT. **c**, Projected density of states (DOS) of the O-2*p* (red) and Te-5*p* (dark yellow) states in DFT-PBE. The Te-5*p* host band comes from fourfold coordinated normal Te^{4+} in TeO_2; the Te-5*p* defect band mainly comes from elemental Te in Te–TeO_x. CB, conduction band. **d**,**e**, Charge density of the Te-5*p* defect band (**d**) and the shallow acceptor state near the Te-5*p* defect band (**e**) in amorphous Te–TeO_x.

channel layer thickness and postannealing temperature affected the TFT performance and, herein, the optimized Se-alloyed Te–TeO_x channel thickness and annealing temperature are around 15 nm and 225 °C, respectively (Extended Data Fig. 6). We noted that an increased applied V_{DS} resulted in increased I_{off} and a positively shifted onset voltage, especially at low Se alloying percentages. This behaviour may arise from the presence of narrow bandgap elemental Te. From the output curves, good current linearity (saturation) was observed at low (high)

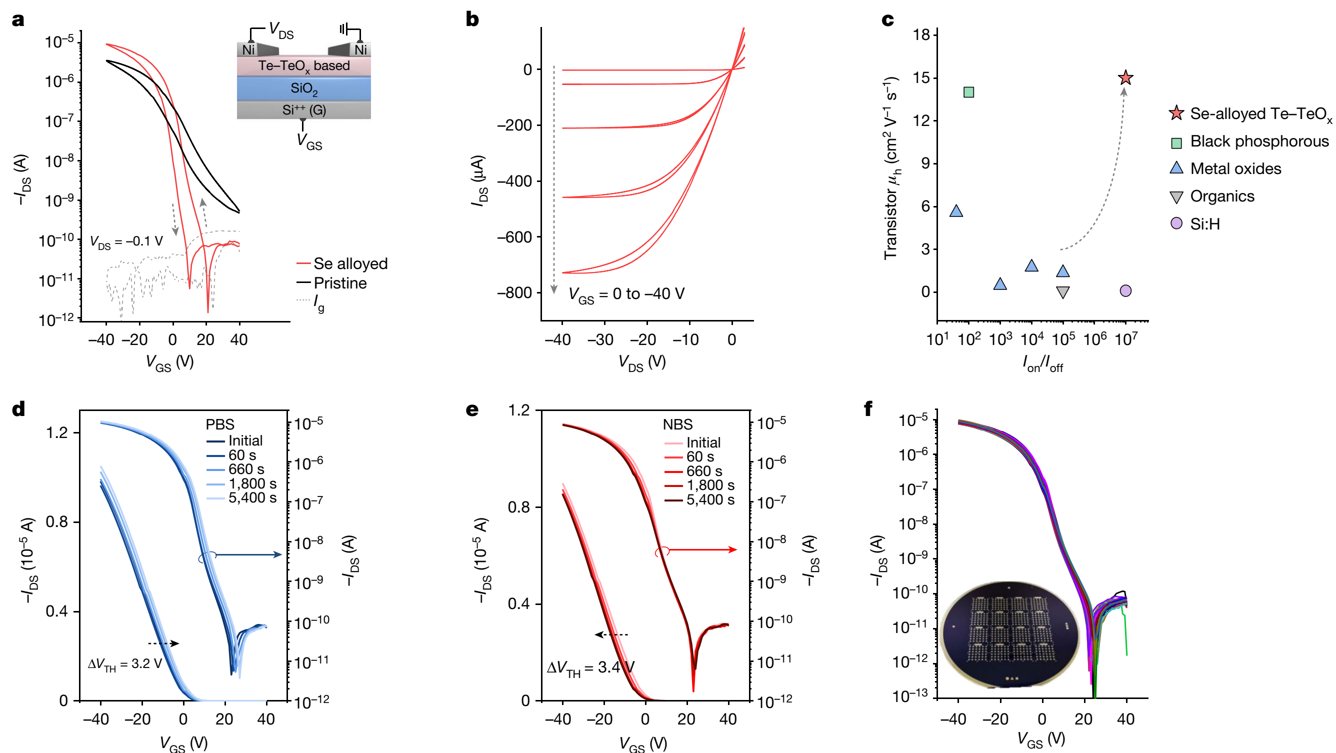

Fig. 3 | Electrical characterizations of amorphous p-channel Se-alloyed Te–TeO_x TFTs on a 100 nm SiO_2 dielectric. a, Transfer characteristics of pristine Te–TeO_x and Se-alloyed Te–TeO_x TFTs; the inset shows TFT geometry (both hysteresis directions are counterclockwise). **b**, Output curves of one Se-alloyed Te–TeO_x TFT. **c**, Benchmark of μ_h and I_{on}/I_{off} of reported amorphous p-channel TFTs. **d**,**e**, Transfer curves and the V_{TH} shifts of Se-alloyed Te–TeO_x TFTs under positive bias stress (PBS) (**d**) and negative bias stress (NBS) (**e**) tests (±20 V) with different time durations. **f**, Transfer curves of 80 randomly measured TFTs fabricated by means of the optimized condition. The inset shows the optical image of TFT arrays on a 10 cm (4 inch) SiO_2 wafer.

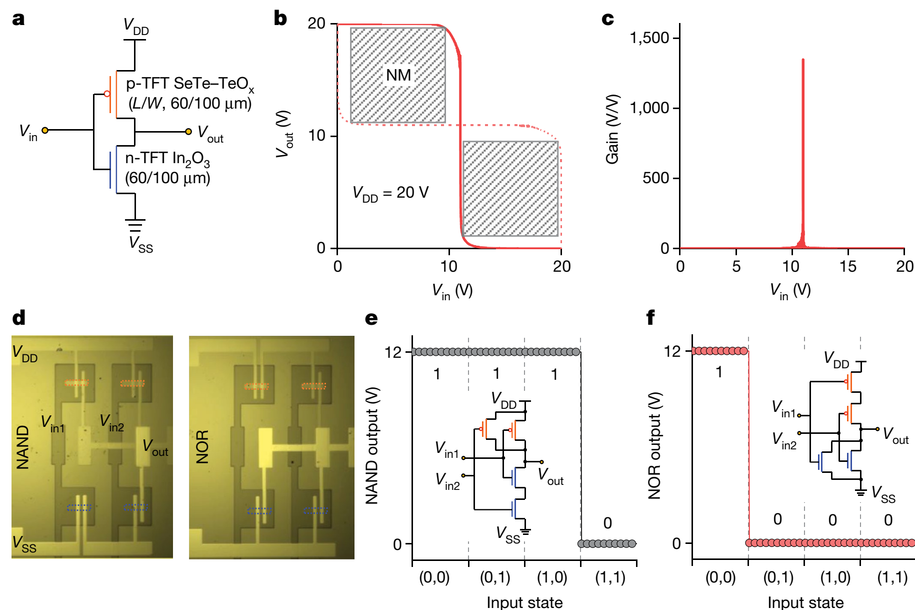

Fig. 4 | Integrated CMOS circuits on a 100 nm HfO_2 dielectric. a–c, Diagram (**a**), voltage transfer, noise margin (NM) extraction (**b**) and gain voltage curves (**c**) of one complementary inverter based on n-channel In_2O_3 and p-channel Se-alloyed Te–TeO_x TFTs at a V_{DD} of 20 V. **d–f**, Photograph (**d**), input and output waveforms for complementary NAND (**e**) and NOR (**f**) logic gates at a V_{DD} of 12 V. The red and blue boxes in **d** indicate the position of p-channel Se-alloyed Te–TeO_x and n-channel In_2O_3 TFTs, respectively. *L*, length; *W*, width.

source-drain voltages, indicating Ohmic contact between the channel layer and electrodes (Fig. 3b). A reasonably low contact resistance of 200 Ω cm was calculated using the transmission-line method[37]. The overall electrical performance surpasses that of p-channel TFTs based on various amorphous semiconductors, such as a-Si:H, organics and metal oxides (Fig. 3c and Extended Data Table 1).

Continuing our exploration, we delved into the Se state and its doping effect on the electrical properties of this amorphous hybrid system. EXAFS analysis confirmed the existence of Se in Se–Te metallic bonds, indicating that the Se was alloyed into the Te in Te–TeO_x (Extended Data Fig. 7). Because of the deeper Se-4*p* state compared to Te-5*p*, the Se alloy can reduce the number of empty 5*p* acceptor states and thus the overall hole conductivity. The fully occupied Se-4*p* orbitals in the valence band can facilitate the filled Te-5*p*-orbital connectivity as well throughout the amorphous network, rationalizing to the enhancement in hole mobilities. The corresponding DFT atomic and band structure are illustrated in Extended Data Fig. 8. Moving on to investigate the device operational stability performance, another critical metric for practical applications, we conducted constant bias stress tests on the Se-alloyed Te–TeO_x TFTs. The results demonstrate decent operational stability, with threshold voltage (V_{TH}) shifts of 3.2 and 3.4 V observed after 5,400 s of positive and negative bias stress tests, respectively (Fig. 3d,e). The negligible variation in the subthreshold region indicated that the Se-alloyed Te–TeO_x channel remained electrically robust during operation, with minimal generation of new defects; the primary instability was attributed to charge trapping[20]. Furthermore, the as-fabricated Se-alloyed Te–TeO_x TFTs showed good ambient durability. Unlike conventional p-type oxide semiconductors, the main composition of metastable cations such as Cu^+ and Sn^{2+} renders them sensitive to oxidation. Other emerging amorphous p-type semiconductors, such as halides and nanomaterials, often face susceptibility to air, impeding their practical applications.

Subsequently, we underscore the processability and scalability of the Se-alloyed Te–TeO_x semiconductor. The channel regions for the aforementioned TFT analysis were patterned using a metal shadow mask to mitigate the gate-leakage current and ensure reliable parameter extraction. We also found the compatibility of Se-alloyed Te–TeO_x channel patterning with standard photolithography, highlighting its feasibility for industrial manufacturing. Further examination of the Se-alloyed Te–TeO_x TFT array over a 10 cm (4 inch) wafer shows high device uniformity and reproducibility (Fig. 3f). The wafer-scale deposition of Se-alloyed Te–TeO_x thin films costs around only US$0.3 for raw powder materials and takes just a few seconds, representing a cost-effective and high-throughput manufacturing process.

Finally, to demonstrate the compatibility of Se-alloyed Te–TeO_x with established n-type metal–oxide technology, we integrated various complementary logic devices, including inverters, NAND gates and NOR gates. An inverter, incorporating n-channel In_2O_3 and p-channel Se-alloyed Te–TeO_x TFTs, showed full-swing characteristics with rapid voltage transitions (Fig. 4a–c). A high voltage gain of 1,300 was obtained at a supply voltage (V_{DD}) of 20 V. The high gain is crucial for signal propagation and logic operations in circuits[38]. The inverter also delivered a high noise margin (82% of $V_{DD}/2$), indicating robust tolerance to noise and input signal variation for cascaded integrated circuit applications. The circuit leakage current as a function of V_{DD} is shown in Extended Data Fig. 9. To enable a lower current level, future efforts could focus on reducing power supply, downsizing TFT and adjusting of the onset voltage of Se-alloyed Te–TeO_x TFT to around 0 V. Two essential logic gates, NAND and NOR, were also constructed, delivering the correct logic function with an ideal rail-to-rail output voltage corresponding to their input states (Fig. 4d–f and Extended Data Figs. 10 and 11).

In conclusion, we have demonstrated high-performance stable p-channel TFTs using amorphous mixed-phase Te–TeO_x-based semiconductors through the scalable thermal evaporation method. The proposed Se-alloyed Te–TeO_x shows superiority over reported emerging amorphous p-type semiconductors, showing outstanding electrical performance, cost-effectiveness, high stability, scalability and processability. The fabrication procedures align seamlessly with industry production lines and back-end-of-line technology. The hybrid-phase strategy introduces a new approach to designing new-generation stable amorphous p-type semiconductors. We expect this study can initiate research topics regarding semiconductor devices and promote the realization and commercialization of cost-effective, large-area, stable and flexible complementary electronic devices and circuits.

Online content

Any methods, additional references, Nature Portfolio reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at https://doi.org/10.1038/s41586-024-07360-w.

1. Nomura, K. et al. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature* **432**, 488–492 (2004).
2. Biggs, J. et al. A natively flexible 32-bit Arm microprocessor. *Nature* **595**, 532–536 (2021).
3. Fortunato, E., Barquinha, P. & Martins, R. Oxide semiconductor thin-film transistors: a review of recent advances. *Adv. Mater.* **24**, 2945–2986 (2012).
4. Yu, X., Marks, T. J. & Facchetti, A. Metal oxides for optoelectronic applications. *Nat. Mater.* **15**, 383–396 (2016).
5. Georgiadou, D. G. et al. 100 GHz zinc oxide Schottky diodes processed from solution on a wafer scale. *Nat. Electron.* **3**, 718–725 (2020).
6. Nathan, A. & Jeon, S. Oxide electronics: translating materials science from lab-to-fab. *MRS Bull.* **46**, 1028–1036 (2021).
7. Si, M. et al. Scaled indium oxide transistors fabricated using atomic layer deposition. *Nat. Electron.* **5**, 164–170 (2022).
8. Portilla, L. et al. Wirelessly powered large-area electronics for the Internet of Things. *Nat. Electron.* **6**, 10–17 (2023).
9. Myny, K. The development of flexible integrated circuits based on thin-film transistors. *Nat. Electron.* **1**, 30–39 (2018).
10. Salahuddin, S., Ni, K. & Datta, S. The era of hyper-scaling in electronics. *Nat. Electron.* **1**, 442–450 (2018).
11. Wang, Z., Nayak, P. K., Caraveo-Frescas, J. A. & Alshareef, H. N. Recent developments in p-type oxide semiconductor materials and devices. *Adv. Mater.* **28**, 3831–3892 (2016).
12. Hu, Y., Yao, X., Schlom, D. G., Datta, S. & Cho, K. First principles design of high hole mobility p-type Sn-O-X ternary oxides: valence orbital engineering of Sn^{2+} in Sn^{2+}-O-X by selection of appropriate elements X. *Chem. Mater.* **33**, 212–225 (2021).
13. Jo, J., Deng, Z., Sanders, N., Kioupakis, E. & Peterson, R. L. Experimental and theoretical study of hole scattering in RF sputtered p-type Cu_2O thin films. *Appl. Phys. Lett.* **120**, 112105 (2022).
14. Liu, J. et al. Effects of Ni doping composition on the physical and electrical properties of $Cu_{1-x}Ni_xO$ thin-film transistors. *IEEE T. Electron. Dev.* **69**, 1092–1098 (2022).
15. Liu, A., Zhu, H. & Noh, Y.-Y. Solution-processed inorganic p-channel transistors: recent advances and perspectives. *Mater. Sci. Eng.: R: Rep.* **135**, 85–100 (2019).
16. Wager, J. F. TFT technology: advancements and opportunities for improvement. *Infor. Disp.* **36**, 9–13 (2020).
17. Paterson, A. F. et al. Recent progress in high-mobility organic transistors: a reality check. *Adv. Mater.* **30**, 1801079 (2018).
18. Xu, Y. et al. Doping: a key enabler for organic transistors. *Adv. Mater.* **30**, 1801830 (2018).
19. Liu, A. et al. High-performance p-channel transistors with transparent Zn doped-CuI. *Nat. Commun.* **11**, 4309 (2020).
20. Liu, A. et al. High-performance inorganic metal halide perovskite transistors. *Nat. Electron.* **5**, 78–83 (2022).
21. Jun, T., Kim, J., Sasase, M. & Hosono, H. Material design of p-type transparent amorphous semiconductor, Cu-Sn-I. *Adv. Mater.* **30**, 1706573 (2018).
22. Liu, A., Zhu, H., Kim, M.-G., Kim, J. & Noh, Y.-Y. Engineering copper iodide (CuI) for multifunctional p-type transparent semiconductors and conductors. *Adv. Sci.* **8**, 2100546 (2021).
23. Das, S. et al. Transistors based on two-dimensional materials for future integrated circuits. *Nat. Electron.* **4**, 786–799 (2021).
24. Peng, L.-M., Zhang, Z. & Qiu, C. Carbon nanotube digital electronics. *Nat. Electron.* **2**, 499–505 (2019).
25. Liu, Y. et al. Promises and prospects of two-dimensional transistors. *Nature* **591**, 43–53 (2021).
26. Choi, S. H. et al. Large-scale synthesis of graphene and other 2D materials towards industrialization. *Nat. Commun.* **13**, 1484 (2022).
27. Zhu, H. et al. Printable semiconductors for backplane TFTs of flexible OLED displays. *Adv. Funct. Mater.* **30**, 1904588 (2020).
28. Liu, A. et al. Evaporated nanometer chalcogenide films for scalable high-performance complementary electronics. *Nat. Commun.* **13**, 6372 (2022).
29. Kim, T. et al. High-performance hexagonal tellurium thin-film transistor using tellurium oxide as a crystallization retarder. *IEEE Electron. Device Lett.* **44**, 269–272 (2023).
30. Kumar, S. & Mansingh, A. Annealing-induced structural changes in tellurium dioxide thin films. *J. Phys. D. Appl. Phys.* **23**, 1252 (1990).
31. Singh, A. & Lessard, R. A. Characterization of evaporated tellurium oxide films. *J. Mater. Sci.* **19**, 3844–3848 (1984).
32. Alderman, O. et al. Short-range disorder in TeO_2 melt and glass. *J. Phys. Chem. Lett.* **11**, 427–431 (2019).
33. Lakshminarayan, N., Radhakrishnan, M. & Balasubramanian, C. Evaporation characteristics of TeO_2 in the formation of tellurium oxide thin films. *J. Mater. Sci.* **21**, 246–250 (1986).
34. Guo, S. et al. Ultrathin tellurium dioxide: emerging direct bandgap semiconductor with high-mobility transport anisotropy. *Nanoscale* **10**, 8397–8403 (2018).
35. Guo, S. et al. High-performance and low-power transistors based on anisotropic monolayer β-TeO_2. *Phys. Rev. Appl.* **17**, 064010 (2022).
36. Zavabeti, A. et al. High-mobility p-type semiconducting two-dimensional β-TeO_2. *Nat. Electron.* **4**, 277–283 (2021).
37. Liu, C., Xu, Y. & Noh, Y.-Y. Contact engineering in organic field-effect transistors. *Mater. Today* **18**, 79–96 (2015).
38. Nomura, K. Recent progress of oxide-TFT-based inverter technology. *J. Infor. Disp.* **22**, 211–229 (2021).

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Methods

Thin-film fabrication and characterizations

TeO_2 (≥97%) and Se (99.99%) powders were purchased from Sigma-Aldrich and directly used as evaporation source. The Te–TeO_x based films were deposited using a thermal evaporator placed in a N_2-filled glove box following a standard procedure to minimize the possible contaminations and vapour toxicity. The mixed TeO_2 (400 mg) and Se (12 mg) powders were loaded in a tungsten boat for optimal conditions. The substrate temperature was maintained at room temperature, and the vacuum pressure before evaporation was around 6×10^{-6} Torr. The distance between the TeO_2/Se powder-loaded tungsten boat and substrate holder was around 20 cm. The thickness of the Se-alloyed Te–TeO_x films was monitored during deposition and the shutter was closed once the desired thickness was obtained. The evaporated samples were annealed at different temperatures for 30 min in ambient air. The crystal structures of the films were analysed using XRD with Cu Kα radiation (Bruker D8 ADVANCE). The HRTEM images and fast Fourier transform patterns were obtained using HRTEM (JEOL JEM 2100F). The X-ray photoelectron spectroscopy analysis was performed using a PHI 5000 VersaProbe instrument (Ulvac-PHI). The Se alloying percentages were characterized using high-resolution inductively coupled plasma mass spectrometry (Thermo Element XR) by dissolving the deposited films in a HNO_3 and HCl mixed acid solvent. Te and Se K-edge X-ray absorption spectra of the Se-alloyed Te–TeO_x films were collected on the BL10C beam line at the Pohang light source (PLS-II) with top-up mode operation under a ring current of 250 mA at 3.0 GeV. Comprehensive measurement details and analysis of X-ray absorption spectroscopy are summarized in the Supplementary Methods (Supplementary Figs. 1–4 and Supplementary Tables 1 and 2).

DFT calculation

The DFT calculations were performed using the Vienna ab initio simulation package code[39]. Projector augmented wave pseudopotentials[40,41] and a kinetic energy cut-off of 500 eV were used. The PBE exchange-correlation functional was used[42]. The amorphous structure was modelled as a cubic supercell using melt-and-quench molecular dynamics simulations. A random initial structure was melted at 3,000 K for 3 ps and then quenched to 0 K at a rate of −1 K fs^{-1}. The residual forces were relaxed to less than 0.01 eV/Å. A single k-point at (1/4, 1/4, 1/4) in the cubic Brillouin zone was used. The molecular dynamics time step was set to 1 fs. The supercell volume was fixed during the molecular dynamics simulations. We generated 50 different $TeO_{1.2}$ amorphous structures (samples) in 79-atom ($Te_{36}O_{43}$) cubic supercells, respectively, using melt-and-quench molecular dynamics simulations beginning with 50 different random initial structures. The calculated properties were the mean values obtained for the 50 samples. The supercell volume was fixed during the molecular dynamics simulations with a lattice constant of 11.6 Å in the cubic supercell.

Device fabrication and characterization

A heavily doped Si wafer (resistivity 1–100 Ω cm) with a 100 nm thermally grown SiO_2 was used as the gate electrode and the dielectric layer. The Se-alloyed Te–TeO_x channels were deposited on SiO_2 as channel layers identically using the aforementioned procedure, followed by the postannealing in ambient air at different temperatures for 30 min. The shadow mask was then covered on the substrate to obtain the patterned channel layers. Ni source and drain electrodes (40 nm) were deposited with a shadow mask using thermal evaporation to construct a bottom-gate top-contact TFT. The channel length and width were 250 and 1,000 μm, unless stated otherwise. All TFT electrical characterizations were characterized using a Keithley 4200 SCS at room temperature in a N_2 glove box. The μ_h was extracted by the McLarty technique in the linear regime. For logic gate integration, a 20 nm Ni was deposited as the patterned gate electrode with a 100 nm atomic-layer-deposited HfO_2 as the dielectric. To prepare the In_2O_3 solution, 0.1 M indium nitrate hydrate was dissolved in 2-methoxyethanol followed by stirring for 3 h. The precursor was spun at 5,000 rpm for 30 s followed by 250 °C annealing for 0.5 h. Thermal evaporated Al was deposited as the source and drain electrode.

Data availability

The data supporting the findings of this study are included within the paper and its Supplementary Information.

39. Kresse, G. & Furthmüller, J. Efficient iterative schemes for ab initio total-energy calculations using a plane-wave basis set. *Phys. Rev. B* **54**, 11169 (1996).
40. Blöchl, P. E. Projector augmented-wave method. *Phys. Rev. B* **50**, 17953 (1994).
41. Kresse, G. & Joubert, D. From ultrasoft pseudopotentials to the projector augmented-wave method. *Phys. Rev. B* **59**, 1758 (1999).
42. Perdew, J. P., Burke, K. & Ernzerhof, M. Generalized gradient approximation made simple. *Phys. Rev. Lett.* **77**, 3865 (1996).
43. Oda, S., Adachi, N., Katoh, S. & Matsumura, M. P-channel amorphous silicon thin-film transistors with high hole mobility. *J. Appl. Phy.* **27**, L1955 (1988).
44. Asada, T. & Koseki, S. Simulation study of hole mobility in the amorphous phase of organic molecules. *Org. Electron.* **53**, 141–150 (2018).
45. Yang, Z. et al. Field-effect transistors based on amorphous black phosphorus ultrathin films by pulsed laser deposition. *Adv. Mater.* **27**, 3748–3754 (2015).
46. Mude, N. N., Bukke, R. N. & Jang, J. High performance of solution-processed amorphous p-channel copper-tin-sulfur-gallium oxide thin-film transistors by UV/O_3 photocuring. *ACS Appl. Mater. Interfaces* **13**, 20277–20287 (2021).
47. Lee, H. J., Lee, S., Lee, K. H. & Hong, K. Amorphous copper iodide: a p-type semiconductor for solution processed p-channel thin-film transistors and inverters. *J. Mater. Chem. C* **10**, 7815–7821 (2022).
48. Xu, W. et al. P-type transparent amorphous oxide thin-film transistors using low-temperature solution-processed nickel oxide. *J. Alloy. Compd.* **806**, 40–51 (2019).
49. Sanal, K. C. & Jayaraj, M. K. Room temperature deposited p-channel amorphous $Cu_{1-x}Cr_xO_{2-\delta}$ thin film transistors. *Appl. Surf. Sci.* **315**, 274–278 (2014).
50. Lee, H.-N., Song, B.-J. & Park, J. C. Fabrication of p-channel amorphous tin oxide thin-film transistors using a thermal evaporation process. *J. Disp. Technol.* **10**, 288–292 (2014).
51. Cheng, X. et al. Amorphous p-type CuNiSnO thin-film transistors processed at low temperatures. *IEEE. T. Electron Dev.* **67**, 2336–2341 (2020).
52. Lu, B. et al. Room-temperature processed amorphous ZnRhCuO thin films with p-type transistor and gas-sensor behaviors. *Chin. Phys. Lett.* **37**, 098501 (2020).

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Author contributions A.L., H.Z. and Y.-Y.N. conceived the study. A.L. performed the experiments and analysed the data. Y.-S.K. performed the DFT calculations. M.G.K. performed the XANES and EXAFS measurements and analysis. H.Z., S.B., Y.R., T.C. and T.Z. assisted with the characterization and discussion. A.L. and H.Z. designed and analysed the circuit. A.L., H.Z., Y.-S.K. and Y.-Y.N. wrote the manuscript. All the authors contributed to the final version of this manuscript.

Competing interests The authors declare no competing interests.

Additional information

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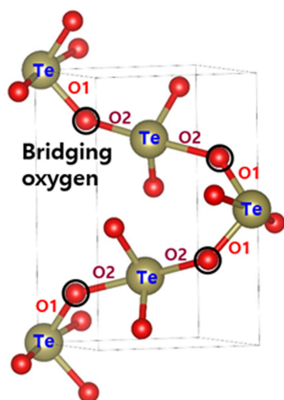

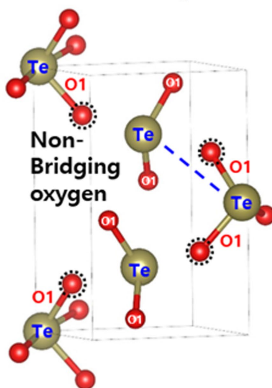

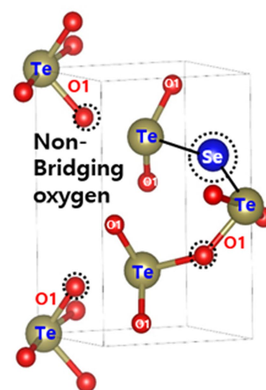

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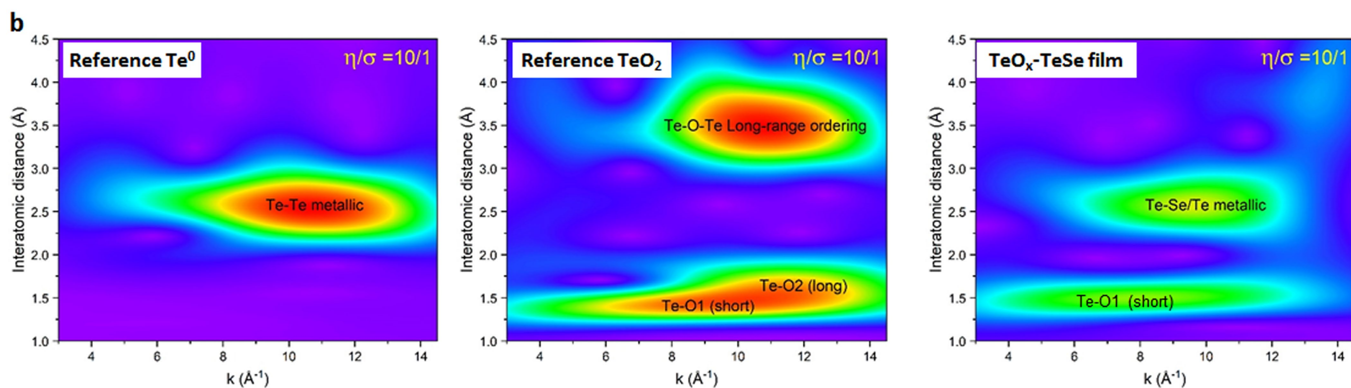
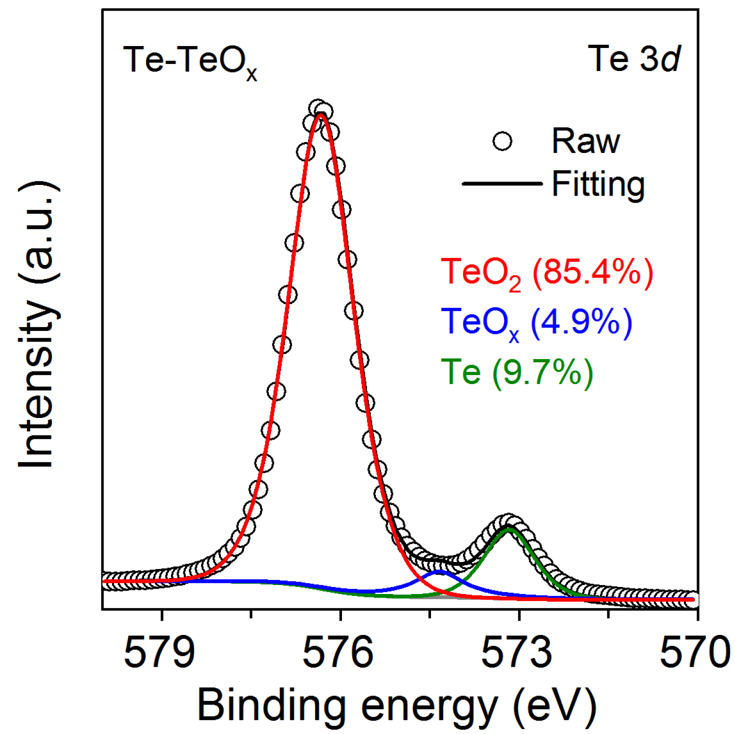
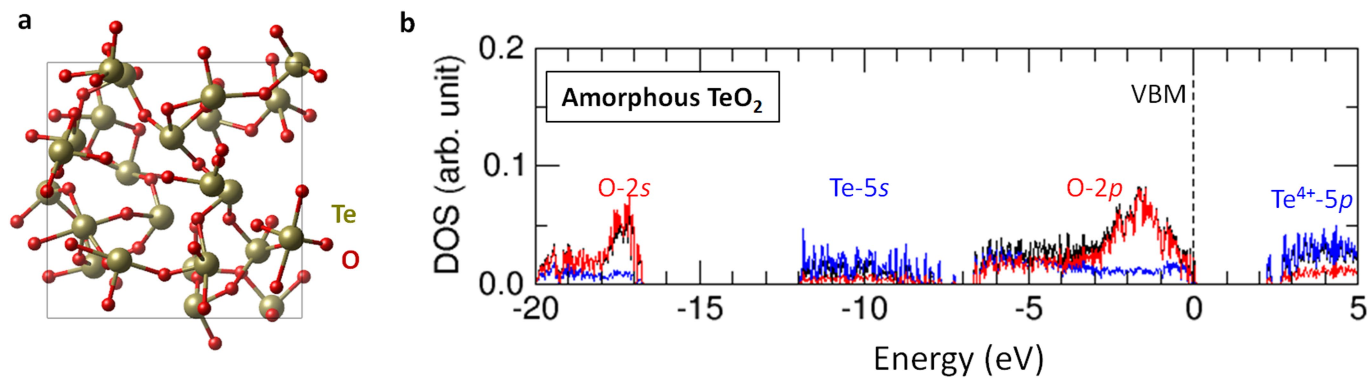


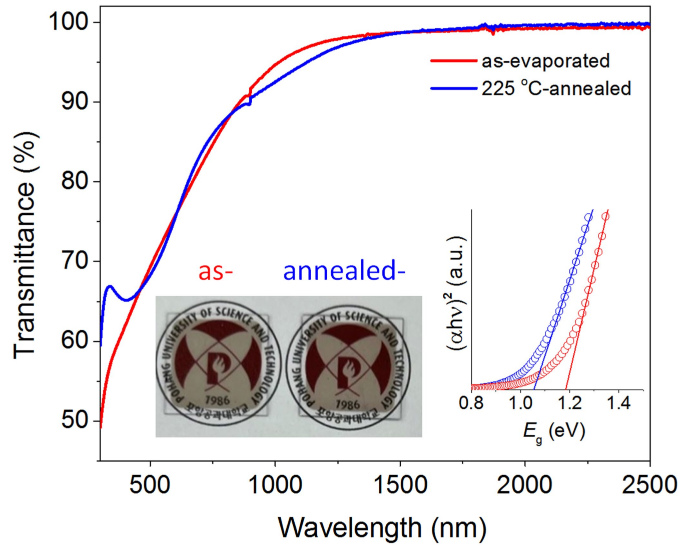
Extended Data Fig. 1 | EXAFS analysis based on different TeO_x models. **a**. Local bonding state of crystalized TeO_2, amorphous sub-stoichiometric Te-TeO_x (longer Te-O2 bond partially broken with the formation of Te-Te metallic bonding), and amorphous Se-alloyed Te-TeO_x (alloyed Se is located at oxygen vacant site with the formation of Te-Se-Te bonding). **b**. Wavelet-transformed *k*-*r* space correlations for EXAFS spectra.



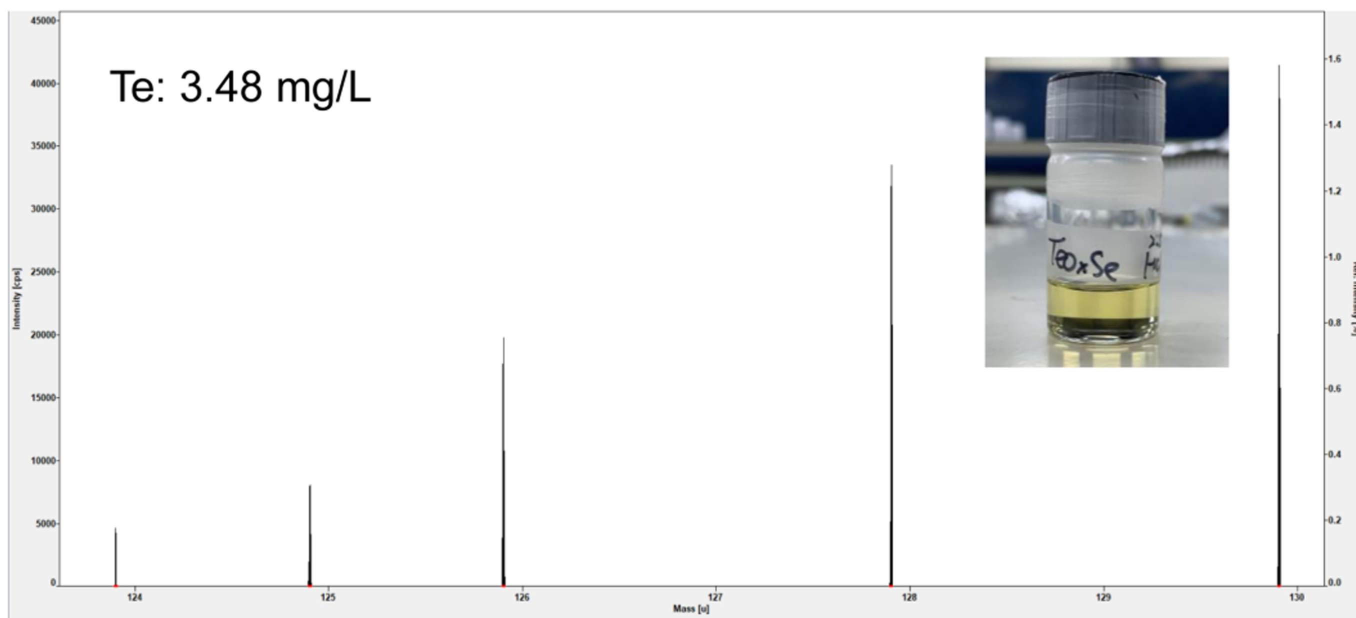
Extended Data Fig. 2 | XPS Te 3*d* spectra of the deposited Te-TeO$_x$ thin film. The XPS measurement was surface scans without etching to avoid the possible influence on the local bonding environment by sputtering.

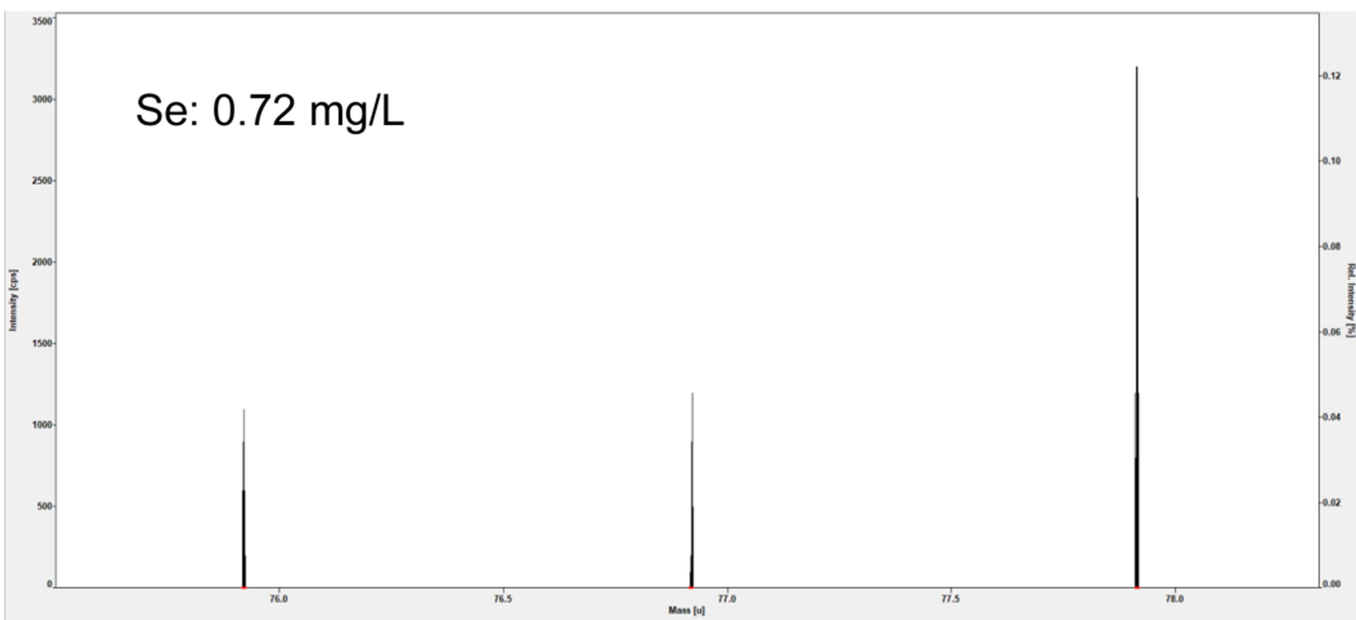


Extended Data Fig. 3 | Atomic and electronic band structures of amorphous tellurium dioxide (TeO_2). **a**. Atomic structure of amorphous TeO_2. **b**. Corresponding local density-of-states, showing the O 2*s*, Te 5*s*, and O 2*p* filled (core or valence) states, and Te^{4+} 5*p* empty (conduction) states.

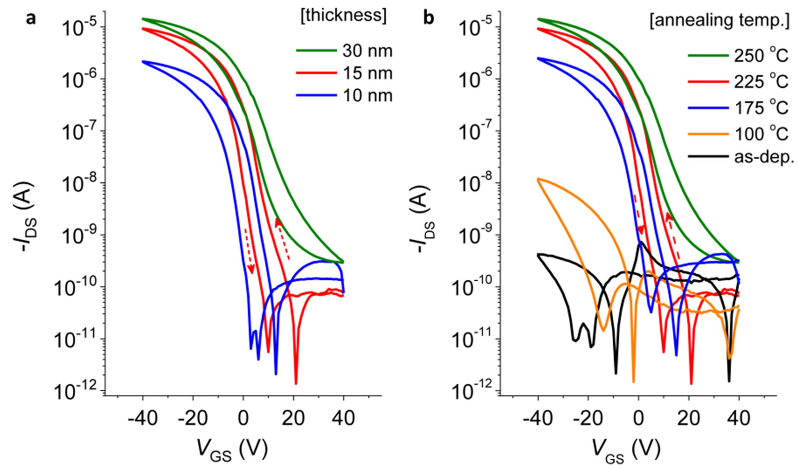


Extended Data Fig. 4 | Optical analysis of the Te-TeO$_x$ thin films. Optical spectra, bandgap extraction, and optical pictures of as-evaporated and 225 °C-annealed Te-TeO$_x$ thin films on glass. The pure TeO_2 was reported to have a wide E_g of ~3.5 eV. In this study, the resulting film consists of a mixed phase of sub-stoichiometric TeO$_x$ and metallic Te. Because of the narrow E_g of Te (~0.35 eV), the final film shows a smaller E_g compared to that of the pure TeO_2.

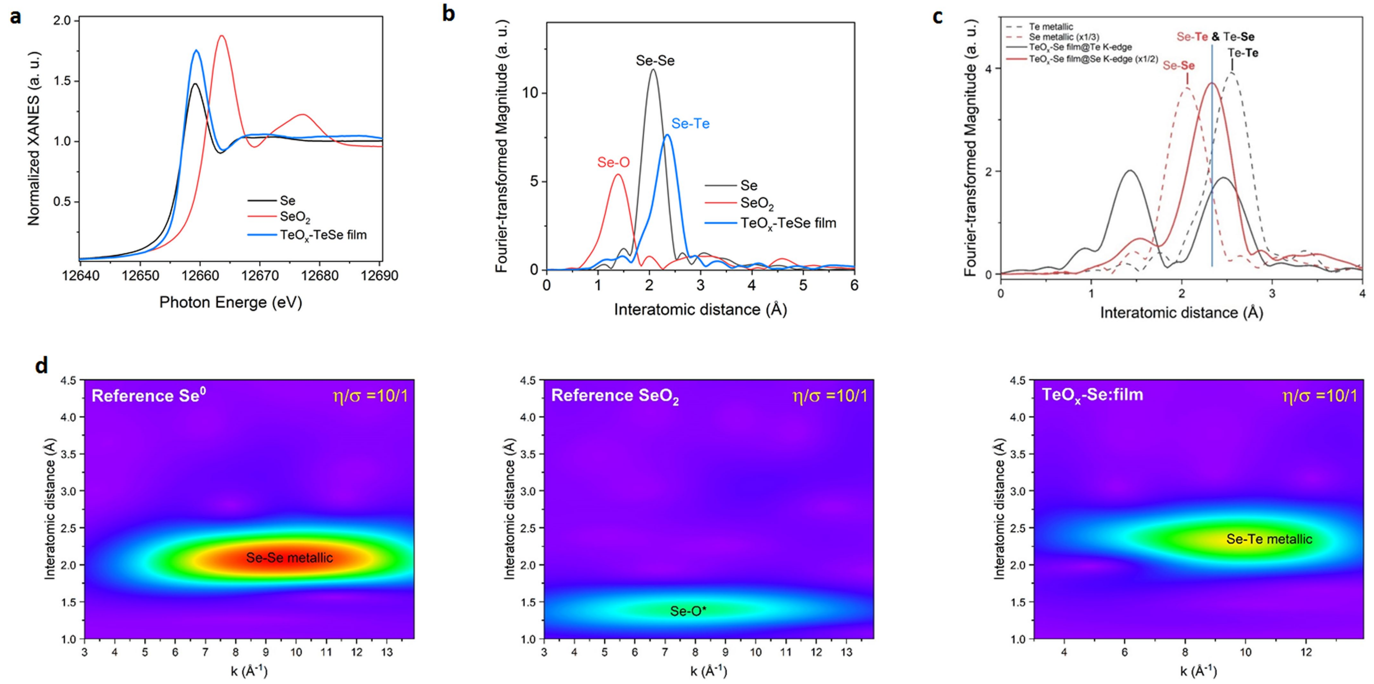




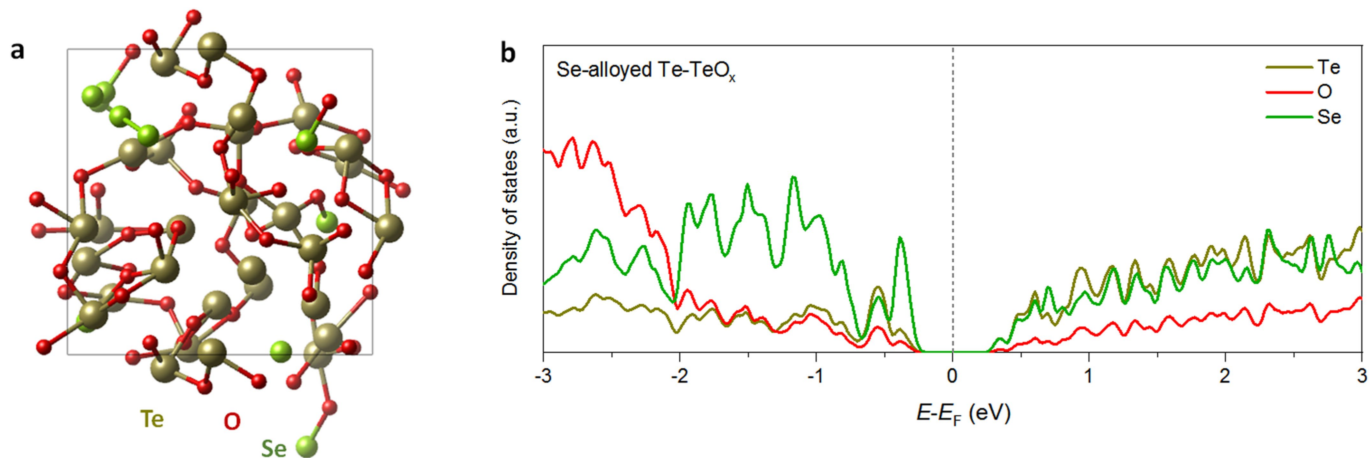
Extended Data Fig. 5 | High-resolution inductively coupled plasma mass spectrometry spectra of Te and Se characterization elements. The inset picture shows the solution used, which is prepared by dissolving the deposited Se-alloyed TeO_x thin film in mixed HNO_3 and HCl acid.



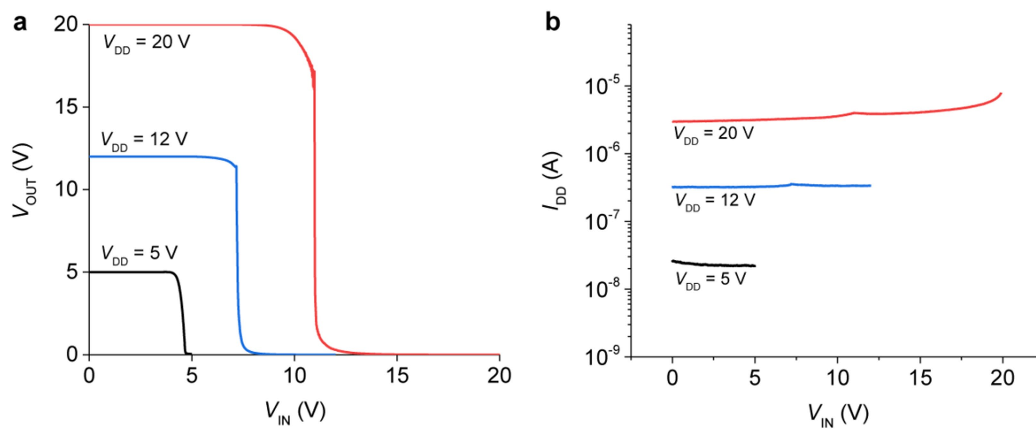
Extended Data Fig. 6 | Transfer characteristics of Se-alloyed Te-TeO$_x$ TFTs with different conditions. a. Transfer curves of Se-alloyed Te-TeO$_x$ TFTs fabricated with different channel thicknesses (channel annealing temperature is 225 °C). **b**. Transfer curves of Se-alloyed Te-TeO$_x$ TFTs deposited with different channel layer postannealing temperatures. All the hysteresis direction is counterclockwise.



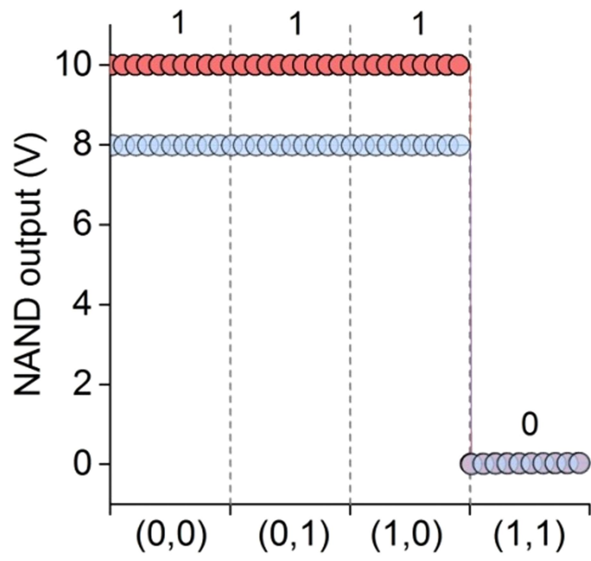
Extended Data Fig. 7 | XANES/EXAFS analysis of on different Te-TeO_x based thin films. **a**. Normalized XANES spectra of the Se-alloyed Te-TeO_x (TeO_x-TeSe) film at Se K-edge, compared to reference materials of Se and SeO_2. **b**. Corresponding Fourier transform (FT) of Se K-edge k^3-weighted EXAFS spectra. **c**. Comparison of Fourier-transformed features for Te K-edge (black solid line) and Se K-edge (red solid line) EXAFS spectra, compared to those of reference metallic Te and Se powder (dashed line). **d**. Corresponding Wavelet-transformed *k*-*r* space correlations for EXAFS spectra of Se, SeO_2, and TeO_x-TeSe film, respectively.



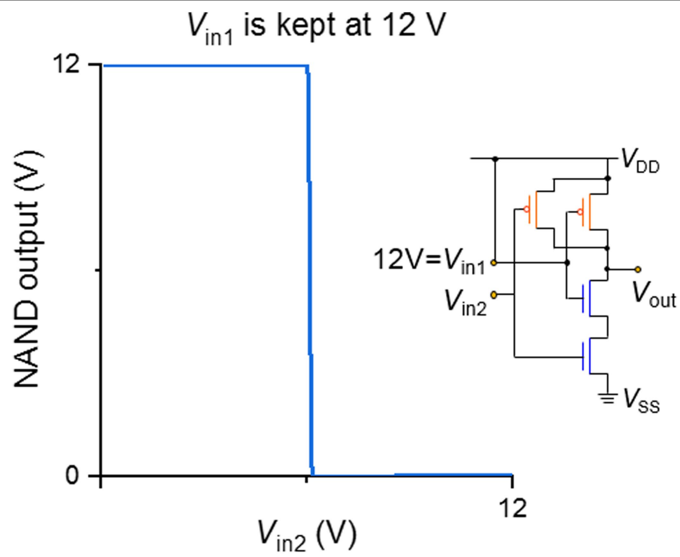
Extended Data Fig. 8 | Atomic and electronic band structures of the Se-alloyed Te-TeO$_x$. **a**. Atomic structure of amorphous Se-alloyed Te-TeO$_x$ generated in DFT (Te:O atomic ratio = 1:1.2; Te:Se atomic ratio = 3:1, film density = 5.6 g/cm^3). **b**. Projected DOS of the O 2*p* (red), Te 5*p* (dark yellow), and Se 4*p* (green) states in DFT-PBE.



Extended Data Fig. 9 | CMOS inverter characterisations. a. Voltage transfer curves of one complementary inverter based on n-channel In_2O_3 and p-channel Se-alloyed Te-TeO_x TFTs at different V_{DD}. **b**. Corresponding circuit leakage current.



Extended Data Fig. 10 | CMOS NAND. The rail-to-rail NAND gate with the working voltage of 10 and 8 V, respectively.



Extended Data Fig. 11 | CMOS NAND with fixed V_{in1}. Plotting of the NAND output *vs* input V_{in2} while V_{in1} was kept at a V_{DD} = 12 V.

Extended Data Table 1 | TFT parameter comparison

Method	Channel material	Annealing temp. (°C)	μ_h ($cm^2 V^{-1} s^{-1}$)	I_{on}/I_{off}	Stability	Ref.
Chemical vapor deposition	a-Si:H	250-350	≤0.1	~10^6	good	43
Solution process/thermal evaporation	Organic	100-150	<0.1	~10^5	poor	44
Pulsed laser deposition	black phosphorus	150	14	~10^2	poor	45
Spin coating	CuSnSGaO	250	1.75	~10^4	--	46
Spin coating	CuI	100	--	~10^4	poor	47
Spin coating	NiO	250	0.48	~10^3	--	48
Sputtering	$CuCrO_2$	150	0.3	~10^4	--	49
Thermal evaporation	SnO	300	5.59	40	--	50
Pulsed laser deposition	CuNiSnO	100	1.37	~10^5	--	51
Magnetron sputtering	ZnRhCuO	RT	0.079	~10^3	--	52
Thermal evaporation	Se-alloyed Te-TeO_x	225	~15	~10^7	good	this work

Representative parameters of p-channel TFTs based on different amorphous p-type semiconductors ("--" means no mention in the reported literature). Refs. 43–52.