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Logic-in-memory application of ferroelectric-based WS_2-channel field-effect transistors for improved area and energy efficiency

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In this study, we applied ferroelectrics to the gate stack of Field Effect Transistors (FETs) with a 2D transition-metal dichalcogenide (TMDC) channel, actively researching for sub-2nm technology node implementation. Subsequently, we analyzed the circuit characteristics of Logic-in-Memory (LiM) operation and utilized LiM features after applying ferroelectrics to achieve a single-device configuration. Based on well-calibrated simulations, we performed compact modeling in a circuit simulator to depict the temperature-dependent electrical characteristics of ferroelectric FETs with a double gate structure and 2D channel (DG 2D-FeFET) in sub-2nm dimensions. Through this, we have confirmed that the 2D FeFET-based LiM technology, designed for the 2 nm technology node, exhibits superior characteristics in terms of delay, power/energy consumption, and circuit area under all temperature conditions, compared to the conventional CMOS technology based on 2D FETs. This verification serves as proof of the future technological potential of 2D-FeFET in extremely scaled-down technology nodes.

CMOS technology scaling down continues, and recent advancements indicate a sustained miniaturization trend with the introduction of 2D transition-metal dichalcogenide (TMDC) materials in the sub-2nm technology node[1]. This trend is anticipated due to the thin TMDC's inherent advantages, such as immunity to short-channel effects, minimal interface trap formation owing to van der Waals bonds and the absence of dangling bonds, excellent mobility characteristics, and superior interface properties compared to silicon[2]. Numerous studies on large-area integration processes and contact technology development for mass production have been reported to facilitate practical implementation[3–5]. Recently, both the IMEC and IRDS CMOS logic technology roadmaps, along with various papers, have provided insights into the feasibility of TMDC in scaled technology nodes[6–8].

Meanwhile, with the increasing prominence of applied research in Artificial Intelligence (AI) and the Internet of Things (IoT), the development of memory-intensive application devices has become crucial. The Von Neumann architecture consists of a Central Processing Unit (CPU), memory unit, and input/output device. The CPU and memory unit exchange data through the system bus. The traditional Von Neumann architecture faces challenges in meeting the requirements of memory-intensive application devices due to the increasing speed difference in data processing between the fast-evolving CPU and memory unit, as well as the unnecessary power consumption escalation in the bus, leading to the Von Neumann bottleneck problem[9–13]. To address such issues, Logic-in-Memory (LiM) research, placing the memory unit and computing core in close proximity, has recently gained momentum[14,15]. LiM can be categorized based on the proximity of the memory unit and computing unit[16]. In-memory computing, processing in memory, and coarse-grain LiM involve Non-Volatile (NV) memory arranged in a matrix array close to the computing core. Fine-grain LiM integrates NV memory tightly with the logic unit within the computing circuit. Recently, circuits such as Full Adder (FA) and Ternary Content Addressable Memory (TCAM) using fine-grain LiM transistors have been reported to exhibit improved circuit area and energy consumption characteristics compared to conventional CMOS FETs[17–20]. FeFETs utilizing the strong ferroelectricity manifested when doping impurities like silicon and zirconium into the hafnium oxide (HfO_2) primarily used as the FET gate insulator have gained significant attention as fine-grain LiM devices. This is attributed to their high compatibility with

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existing silicon-based integration processes. Global Foundries has demonstrated FeFET devices based on 28 nm CMOS and 22 nm FDSOI CMOS as baseline FETs, along with various application circuit results[21].

In previous studies, the resistance and capacitance of FETs with a channel made of TMDC material were segmented, and an analysis based on the number of channel layers was conducted[2,22]. However, there is currently a lack of preliminary research on analyzing the characteristics of devices by depositing a strong ferroelectric on 2D materials. In this paper, we modeled a DG FeFET by integrating one of the representative 2D TMDC materials, tungsten disulfide (WS_2) channel, with a ferroelectric, 10 nm HSO, in the sub-2nm dimension. We predicted the device and LiM circuit characteristics. To achieve this, we extracted the electrical characteristics of DG FeFET devices by utilizing the electrical properties of WS_2 channels in DG FETs, calculated through atomic-level simulations by Ahmed et al., and the electrical characteristics of a Silicon-doped hafnium oxide (HSO) ferroelectric layer reported from fabrication devices by Zhou et al.[23,24]. We developed a compact model that describes this process and benchmarked power, performance, and area characteristics in various FA and TCAM circuits through circuit simulations. In this process, we utilized a conventional FA circuit (1 type) and TCAM circuit (1 type) composed of DG FETs, along with two previously published FeFET-based FA circuits (2 types) and TCAM circuits (2 types), and a proposed FeFET-based FA circuit (1 type) in this paper. Additionally, we confirmed robust circuit operation characteristics in nano-scale nodes through circuit characteristic verification under various temperature conditions. The structure of this paper is as follows. In Chapter 2, we describe the circuit modeling method, including the electrical characteristics of the WS_2 channel and ferroelectric layer used in the DG FeFET in this study, as well as temperature variations. In Chapter 3, we perform various FA and TCAM circuit analyses and benchmarks using the developed DG FeFET's LiM characteristics. In particular, we evaluate circuit layout area comparisons and circuit robustness against temperature changes. Finally, in Chapter 4, we conclude the paper.

Results

Characteristics of DG FeFET with Mono-layer WS_2 channel and HSO ferroelectric layer

Figure 1 illustrates the double-gate structure of a 2D-channel FeFET with a monolayer WS_2 channel and a ferroelectric gate dielectrics, as employed in this study. Table 1 outlines the key dimensions applied to the 2D-channel DG FeFET structure in this research, corresponding to sub-2nm technology node dimensions[6]. In particular, the thickness of the ferroelectrics and dielectrics is an important factor in the capacitance characteristics (C_{FE}/C_{DE}) that determine the memory window (MW). 2D-based FET exhibits advantages over Si-based FET in scaling aspects in the latest processes, and it is evident that they possess superior electrical properties.

Compact modeling of DG FeFET with Mono-layer WS_2 channel and HSO ferroelectric layer

In Fig. 2, the summarized development process of the overall FeFET compact model library for LiM-based FA and TCAM circuit analysis is presented. As illustrated in Fig. 3, this study employs a Metal-Ferroelectric-Insulator-Semiconductor (MFIS) structure FeFET, integrating a ferroelectric layer into the gate stack of the baseline FET. This integration was implemented using the principles of charge conservation and voltage distribution. In the absence of metal between ferroelectrics and dielectrics, polarization coupling occurs, exerting a slight influence on the overall capacitance[28]. However, simulations were conducted under the assumption of no polarization coupling, representing an ideal scenario. The self-developed ferroelectric device model, implemented in Verilog-A, was integrated into the baseline FET using BSIM-IMG, and the electrical characteristics of the FeFET were simulated through Synopsys' HSPICE. The obtained Memory Window with applied Program/Erase voltage, as determined by the FeFET compact model, is summarized in Fig. 3.

The development process of a compact model library for WS_2-based FET used as the baseline FET is included in Fig. 2, steps ①-②. In this study, results based on atomic-level simulations of WS_2 channels, deemed capable of achieving sub-2nm, were utilized. To verify the dynamic characteristics of the circuit, *I–V* calibration was performed using the standard TCAD software, Synopsys's Sentaurus, followed by obtaining C-V characteristics. We used the thin layer model for WS_2-FET with a channel thickness of a few nm, and included the IALmob model to describe surface and phonon scattering, and the RCS model to represent remote coulomb scattering due to high-k gate dielectrics. Subsequently, for the development of the compact model library for the baseline WS_2-based FET, the industry-standard BSIM-IMG model suitable for Double Gate structures was utilized. Initially, process variables were utilized as the physical parameter set. Parameters describing electrical characteristics such as *I–V* and *C–V* at $T = 300$ K were extracted, while temperature-dependent parameters were extracted at $T = 230$ K and 360 K, respectively. In the circuit simulation netlist, the parasitic components (C_{EXT}, C_{MOL}, R_{EXT}, R_{MOL}) and contact resistance (R_{CNT}) that affect the AC condition were connected to the WS_2-FET as shown in Fig. 4a to analyze the circuit performance. C_{EXT}, C_{MOL}, R_{EXT}, R_{MOL} were obtained from well-calibrated TCAD, while R_{CNT} at 300 K (=1.8 kΩ μm) was reported from experiments[23], and R_{CNT} at 230 K and 360 K were taken from experimental values in Li et al.[29]. Subsequently, I_{off} targeting and centering were performed to meet the speed and power requirements of the sub-2nm node as per the industry standards.

Figure 5 outlines the compact modeling process for the characteristics of the 10 nm ferroelectric layer used in this study. It is a model that integrates formulas that describe various physical characteristics of various ferroelectric layers in previous studies into one[24,30,31]. Verilog-A is used to output polarization characteristics by voltage values input over time on circuit simulators. Equation 1 describes the saturation loop of the ferroelectric layer, while Equations 2–4 depict the nonsaturated inner loop characteristics. Equation 5 represents the total polarization, including dielectric characteristics, and Equations 6–8 describe the temperature-dependent properties. In Equation 6, the temperature dependence of the saturation polarization of the ferroelectric capacitor is assumed to follow Landau theory. Equation 7 utilizes the approximation that the coercive field is considered when the temperature (T) is lower than the Curie's temperature (T_C)[32]. Energy barriers (W_B), Boltzmann constant (k_b), potential barrier height (v_0), Critical Volume (V^*), Saturation Polarization (P_S), and the time

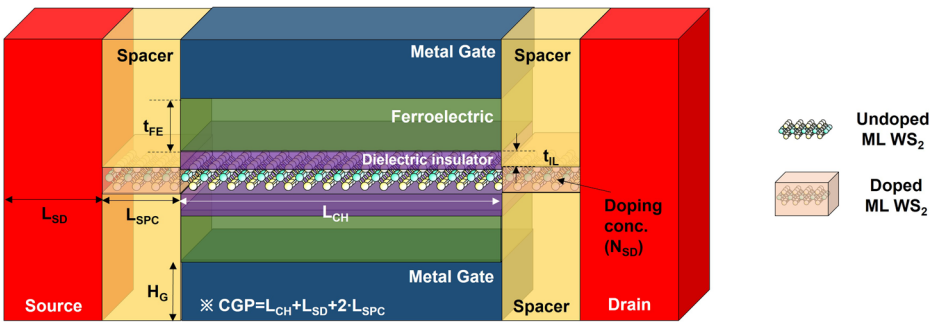


Fig. 1 | 2D-channel Double Gate FeFET structure with monolayer WS_2 channel and ferroelectric gate dielectrics used in this study.

Table 1 | Key device parameters for 2D-channel DG FeFET used in this work to describe sub-2nm technology node

Parameter		Channel materials – Technical node		
		Si FinFET - 3 nm	Si GAAFET - 2 nm	WS_2 DGFET - Sub-2nm (this work)
Dimension	Contacted poly-gate pitch (CGP)	48 nm	45 nm	42 nm
	Metal pitch (MP)	24 nm	20 nm	16 nm
	Gate length (L_G)	16 nm	14 nm	14 nm
	Channel width (W_{CH})	101 nm	216 nm	52 nm
	Spacer length (L_{SPC})	6 nm	6 nm	8 nm
	Source/Drain contact length (L_{SD})	20 nm	19 nm	12 nm
	Interfacial layer thickness (T_{IL} or EOT)	0.5 nm	0.5 nm	0.5 nm
	Source/Drain extension region doping concentration	10^{21}–10^{22} cm^{-3}	10^{21}–10^{22} cm^{-3}	4×10^{20} cm^{-3}
	Spacer dielectric constant	3.5	3.3	7.5
	Interfacial layer dielectric constant	3.9	3.9	3.9
Electrical property	Supply voltage (V_{dd})	0.70 V	0.65 V	0.5 V
	Effective Mobility	125 $cm^2/V{\cdot}s$	100 $cm^2/V{\cdot}s$	200 $cm^2/V{\cdot}s$
	On current	874 μA/μm	787 μA/μm	1.1 mA/μm
	Contact resistance @ 300 K	1×10^{-9} Ω cm^2	1×10^{-9} Ω cm^2	1.8 kΩ μm

The benchmark results of Si-based FET and 2D-based FET in the latest processes are included[6,7,23–27].
Ferroelectric layer thickness (T_{FE}): 10 nm

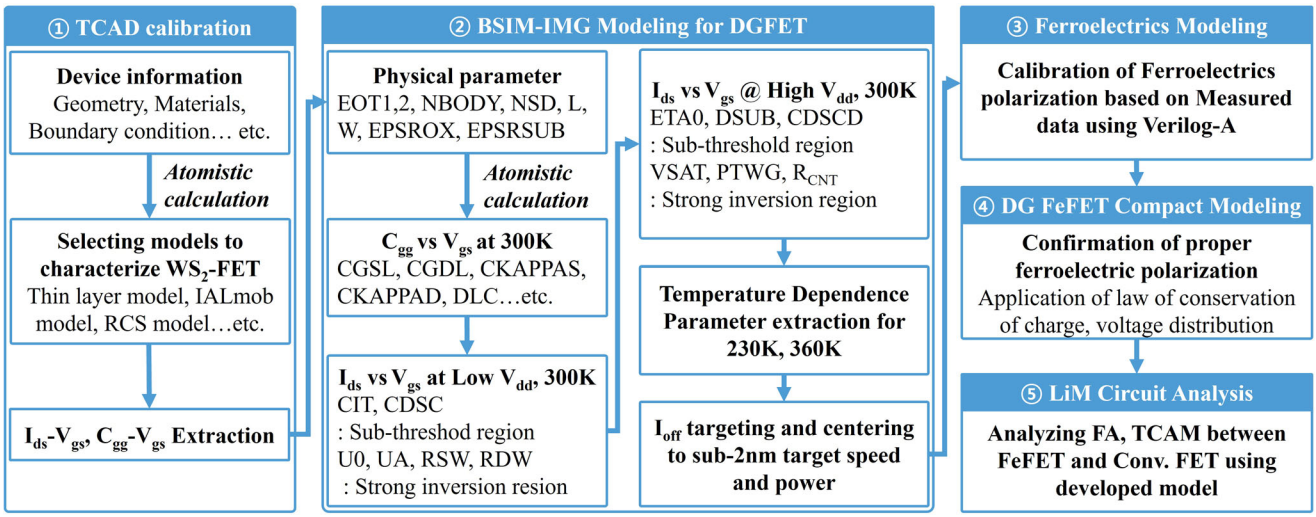
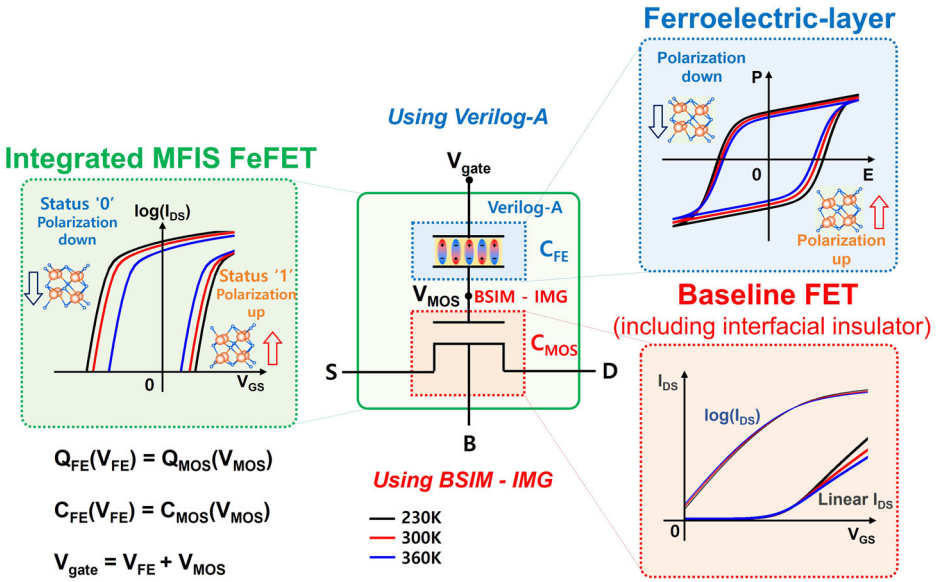


Fig. 2 | Overall process flow for Mono-layer WS_2 channel DG FeFET from TCAD simulation to LiM circuit benchmarking.

taken for Coercive field (E_C) is a known constant, so E_C and Temperature (T) have a linear relationship. This led to the derivation of Equation 8 applying Vopsaroiu's model. Here, V_C represents the coercive voltage, $P_{\uparrow\downarrow}(V_{EFF})$ represents the polarization of the inner loop, ε_{FE} is the dielectric constant of the ferroelectric material, ε_0 is the dielectric constant in the air, t_{FE} is the thickness of the ferroelectric material, $P_{S,0K}$ is the saturation polarization at absolute temperature, T_{EFF} is the absolute temperature of the current state, and A and B are fitting parameters for determining E_C concerning temperature. The model, considering hysteresis and the non-saturated inner loop, is expressed using Verilog-A following the flowchart in Fig. 5 to implement ferroelectric spontaneous electric polarization. Figure 5 provides a detailed explanation of step 2 in Fig. 2. The Verilog-A describing the ferroelectric capacitor is divided into sections for the temperature impact and the part related to ferroelectric hysteresis. First, ε_{FE}, t_{FE}, which are ferroelectric material information, P_S, a, and V_C of Equation 1 are set for polarization according to temperature conditions. After that, if it is not room temperature, P_S and V_C are corrected for the current temperature through Equation 6-8. Ferroelectric hysteresis is described after P_S, V_C calibration. When in the saturation loop, $m = 1$ and $b = 0$ in Equation 2, and in the non-saturated inner loop, Equation 3 and 4 are used to calculate m and b in Equation 2. The equivalent circuit of the ferroelectric layer (FeCAP) modeled based on Equations 1–8 consists of R_{FE}, C_{FE}, and C_0, as shown in Fig. 6c, enabling the description of dynamic response. The charge density (Q) of FeCAP arises from spontaneous polarization (P) and induced displacement due to the permittivity of the ferroelectric layer ($\varepsilon_{FE}\varepsilon_0$) (Equation 5). The variation of P with applied voltage is modeled by C_{FE}, while the linear displacement component is modeled by C_0. Here, R_{FE} is introduced to delay the charging of C_{FE}, describing the RC delay ($\tau_{FE} = R_{FE}C_{FE}$) in polarization switching.

FA and TCAM design based on FeFET and circuit analysis

The Power Performance Area characteristics of fully WS_2-FET-based FA and TCAM, as well as partially WS_2-FeFET-utilized FA and TCAM, were benchmarked. In all operations, the Program/Erase voltage is set to 2 V, and



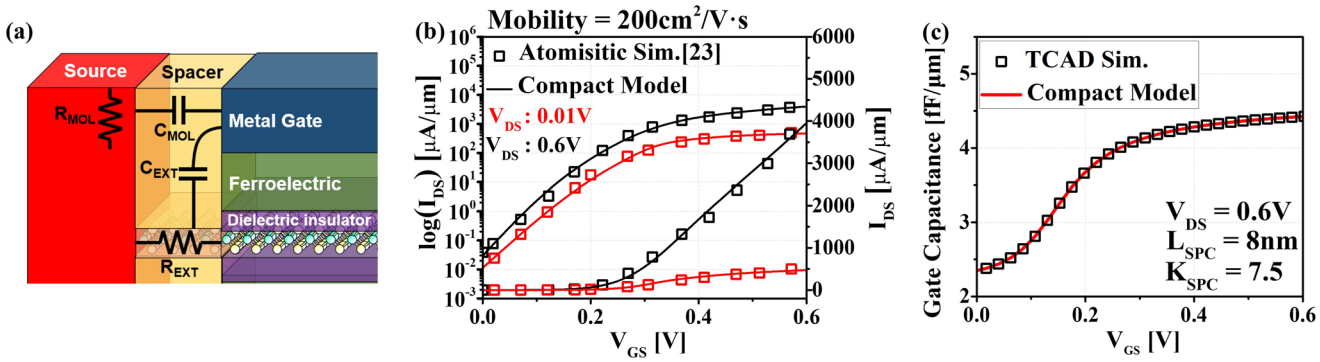


Fig. 3 | Overall description of FeFET and equations for developing a FeFET compact model.

Fig. 4 | Parasitic components and intrinsic characteristics of WS_2 DG FET considered in this study to perform circuit-level benchmarks. a Capacitances, resistances of MOL, extension, **b** Intrinsic *I*–*V* graph of DG WS_2-FET with high voltage (V_{ds} = 0.6 V), low voltage (V_{ds} = 0.01 V), **c** Intrinsic gate capacitance graph for high voltage[22].

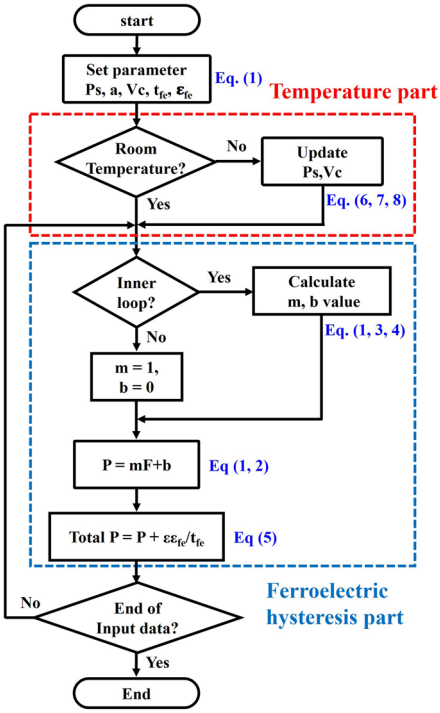
the input voltage is set to 0.5 V. The transistor count for FA varies, with the 28 T FA having the highest count at 28 transistors, the 3 FeFETs FA having the lowest count at 19 transistors, and the 6 FeFETs FA having 21 transistors. The FeFET TCAM include a 2 T 2FeFETs TCAM with four transistors and a 2FeFETs TCAM with 2 transistors. FeFETs TCAM replace 6 T SRAM in the 16 T TCAM with NV memories. Both FeFET-based FA and TCAM use fewer transistors than conventional FA and TCAM, providing an advantage in terms of spatial efficiency. Supplementary Table 1 presents the input waveform conditions and transistor counts for the 28 T, 3 FeFETs, 6 FeFETs FA, and 16 T, 2 T 2FeFETs, 2FeFETs TCAM.

In Supplementary Fig. 1, the design of the 28 T FA takes advantage of the complementary connection of nMOS and pMOS. The serial connection of nMOS is convertible to the parallel connection of pMOS, and vice versa. Unlike 28 T FA, the 3FeFETs FA proposed by Yin et al. using FeFET does not work complementarily with nMOS and pMOS, and consists of nMOS except for clock transistor and inverter transistor[19].

As seen in Fig. 6c, in the Polarization up (P-up) state, the output is 1, and in the Polarization down (P-down) state, the output is either 1 or 0. The 6FeFETs FA is a designed structure based on the array structure proposed by Breyer et al.[33]. In Breyer et al.'s study, an FA using FeFETs requires an FeFET *I*–*V* curve that outputs 1 or 0 when P-up and 0 when P-down. Therefore, the curve needs to be shifted to the right, which poses challenges such as delay time issues when using the different type of *I*–*V* curve. In order to use the curve in the form of Fig. 6c without moving, 6FeFETs FA was designed in this paper. Unlike the 3FeFETs FA, Sum and C_{OUT} operate independently. Sum is obtained through XOR gates, and C_{OUT} is calculated using AND gates. The structure is arranged in a NOR memory array format, which does not interfere with FeFET switching, making write operations easy. It can be applied to various array structures, such as memristor-crossbar memory arrays. The incorporation of nonvolatile devices' write operations in existing logic FA can lead to abrupt voltage/current drops. By integrating non-volatile characteristics into volatile circuit structures, a stable LiM structure with nonvolatility is achievable. Two clock transistors and four inverter transistors are connected to the bit line.

The I_d–V_g curves for 3 FeFETs, 6 FeFETs FA at 230 K, 300 K, and 360 K can be observed through Fig. 6c. The read voltage for both 3 FeFETs and 6 FeFETs FA is set to 0.5 V. As shown in Supplementary Fig. 1e-h, applying 2 V stores 1 in the FeFET, and it continues to operate with the value 1. When −2 V is applied, 0 is stored in the FeFET. The 28 T, 3FeFETs, and 6FeFETs FA operate similarly at 230 K and 360 K.

In the analysis of circuit characteristics such as Delay time, Dynamic Power, Standby Power, and Power Delay Product (PDP) for circuits based on 28 T, 3FeFETs, and 6FeFETs FA at different temperatures, the results were summarized in Supplementary Table 2 and Fig. 7. In all aspects, the 6FeFETs FA outperformed others. When compared to the 28 T FA for Delay time, the 3FeFETs FA improved by 12.7%, and the 6FeFETs FA improved by 16.8%. In the WS_2-FET I_d–V_g curve of the 28 T FA, the I_{on}/I_{off} was lower than that of the 3FeFETs FA, leading to an improvement in Delay time for the 3FeFETs FA over the 28 T FA. Unlike the 28 T FA, which passes through three transistors



$$F_{\uparrow\downarrow}(V_{EFF}) = P_S \tanh[a(V_{EFF} \pm V_C)] \quad (1)$$

$$P_{\uparrow\downarrow}(V_{EFF}) = mF_{\uparrow\downarrow}(V_{EFF}) + b \quad (2)$$

$$m = (P_{\uparrow\downarrow}(V_{i+1}) - P_{\uparrow\downarrow}(V_i)) / (F_{\uparrow\downarrow}(V_{i+1}) - F_{\uparrow\downarrow}(V_i)) \quad (3)$$

$$b = \frac{(P_{\uparrow\downarrow}(V_i)F_{\uparrow\downarrow}(V_{i+1}) - P_{\uparrow\downarrow}(V_{i+1})F_{\uparrow\downarrow}(V_i))}{(F_{\uparrow\downarrow}(V_{i-1}) - F_{\uparrow\downarrow}(V_i))} \quad (4)$$

$$P_{TOTAL} = P_{\uparrow\downarrow}(V_{EFF}) + \varepsilon_{FE}\varepsilon_0 / t_{FE} \quad (5)$$

$$P_S = P_{S,0K}\sqrt{\frac{T_C - T_{EFF}}{T_C}} \quad (6)$$

$$E_C(t, T) \simeq \frac{W_B}{P_S} - \frac{k_b T}{V^* P_S} \ln\left(\frac{v_0 t}{\ln(2)}\right) \quad (7)$$

$$E_C = (A + B(T_{EFF})) / t_{FE},\ V_C = E_C t_{FE} \quad (8)$$

Fig. 5 | Process flow developed using Verilog-A code for describing temperature and hysteresis characteristics of ferroelectric layer.

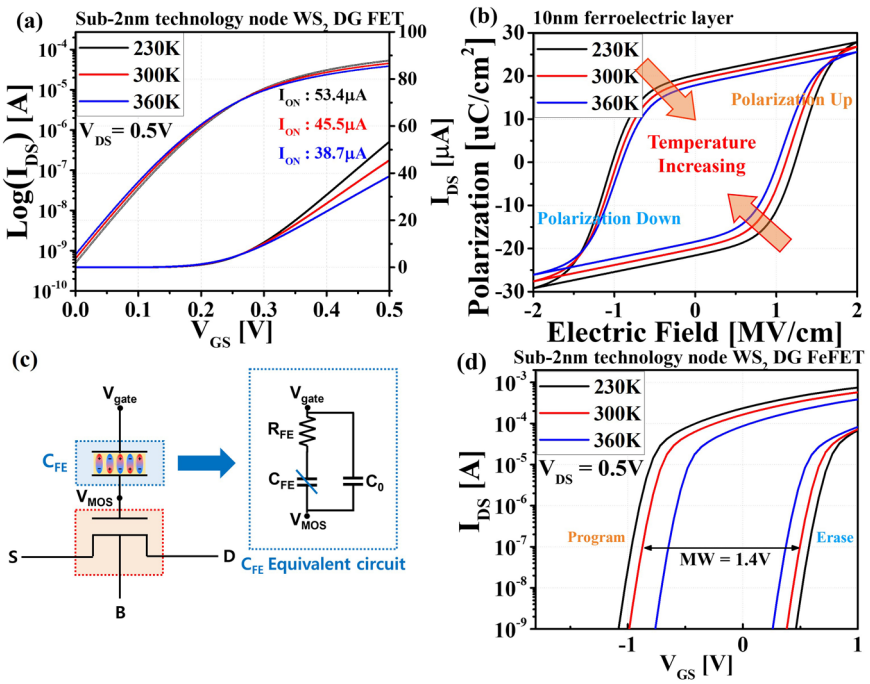


Fig. 6 | Compact modeling overview addressing parasitic components, contact resistance of DG WS_2-based FET, and dynamic response characteristics of ferroelectrics. a WS_2-FET temperature-dependent I_d–V_g curve considering contact resistance, **b** Ferroelectrics temperature-dependent polarization-electric field hysteresis curve, **c** Ferroelectric model connected in series with R_{FE} and in parallel with linear capacitor, **d** Temperature dependent measured I_d–V_g curve of WS_2-FeFET. Note that the Memory Window of 1.4 V is obtained through Program (PG) and Erase (ER) states at 300 K, including contact resistance characteristics. This has a great advantage in terms of Memory operation.

from input to output, the 6FeFETs FA passes through approximately two WS_2-FETs, resulting in the smallest Delay time characteristic. Dynamic Power improved by 29.1% for the 3FeFETs FA and 57.7% for the 6FeFETs FA. The 28 T FA utilizes all 28 transistors during operation, while the 3FeFETs FA uses all 19 transistors as the output of !C_{OUT} is used as an input for Sum operation. Additionally, FeFET has a high I_{on}/I_{off}[19]. Therefore, the Dynamic Power of the 3FeFETs FA is lower than that of the 28 T FA. In contrast to the 3FeFETs FA, which operates with complex interactions between Sum and C_{OUT}, the proposed 6FeFETs FA operates in array form where Sum and C_{OUT} operate independently. When C_{IN} is 1, 13 transistors operate, and when C_{IN} is 0, 14 transistors operate. The 6FeFETs FA, with the fewest operating transistors, has the lowest Dynamic Power, followed sequentially by the 3FeFETs FA and the 28 T FA. Supplementary Fig. 2a, b illustrates the proportion of power taken by FeFET and WS_2-FET in the Total Dynamic Power of 3FeFETs and 6FeFETs FA. Looking at the Dynamic Power per transistor, in the 3FeFETs FA, FeFET accounts for 0.4%, and WS_2-FET accounts for 6.2%. In the case of the 6FeFETs FA, FeFET accounts for 0.9%, and WS_2-FET accounts for 6.3%. This indicates that the Power consumed by FeFET is significantly small, and there is an

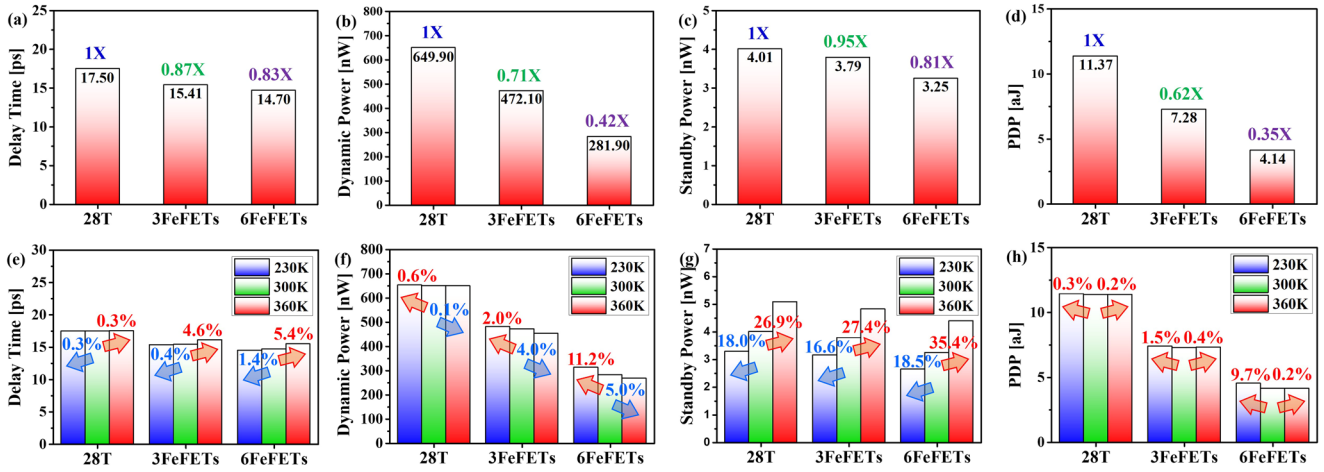
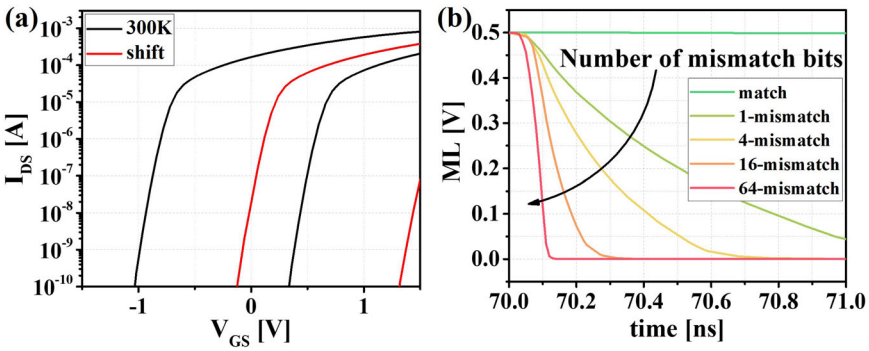


Fig. 7 | Time-dependent results of FA. a, **e** Delay time, **b**, **f** Dynamic Power, **c**, **g** Standby Power, **d**, **h** PDP of FA. The values in (**a**–**d**) are taken from 300 K in Supplementary Table 2.

Fig. 8 | *I*–*V* Curve and number of mismatch bits characteristics for 2FeFETs TCAM operation. **a** *I*–*V* hysteresis graph with V_{th} shifted to the right, **b** The variation of the ML node with an increase in number of mismatch bits (64 × 64 size).



advantage in Power as the number of FeFETs increases. Standby Power improves by 5.5% for the 3FeFETs FA and 19.0% for the 6FeFETs FA. The 28 T FA has the highest Standby Power because it has more transistors than the 3FeFETs and 6FeFETs FA. 6FeFETs FA has more transistor counts than 3FeFETs FA, but 6FeFETs FA has the lowest Standby Power because the circuit of 6FeFETs FA has more parallel structures than 3FeFETs FA. PDP improves by 38.1% for the 3FeFETs FA and 64.8% for the 6FeFETs FA. Ultimately, the 6FeFETs FA, with the smallest Delay time and lowest Dynamic Power, exhibits the best PDP characteristics.

Figure 7e–h depicts circuit characteristics at temperatures of 230 K, 300 K, and 360 K. Delay time improves as the temperature decreases. For Dynamic Power, it increases as the temperature decreases. In Fig. 6a, the I_{on} of the 2D-channel DG FET used as the Baseline FET increases in the order of 230 K, 300 K, and 360 K. Therefore, Delay time is directly proportional to temperature, while Dynamic Power is inversely proportional to temperature. Standby Power improves as the temperature decreases. Since I_{off} increases in the order of 360 K, 300 K, and 230 K, Standby Power is directly proportional to temperature. At all temperatures, the Delay time of the 6FeFETs FA is the shortest compared to the 28 T FA, and Dynamic Power and Standby Power also decrease the most in the 6FeFETs FA. Consequently, the Delay time, Dynamic/Standby Power, and PDP characteristics of the 6FeFETs FA are the most superior.

As shown in Supplementary Fig. 3, Supplementary Table 3, to compare the circuit layout area of FA, we designed the Layout Versus Schematic (LVS) process directly. For layouts targeting sub-2nm technology nodes, a 42 nm CGP and a 16 nm MP were employed. The circuit area of the 3FeFETs FA, considering metal wiring, improved by 22.9% compared to the 28 T FA. The circuit area of the 6FeFETs FA decreased by 13.1% compared to the 28 T FA. The 3FeFETs FA, with the fewest transistor counts, has the smallest area. Therefore, the use of FeFETs results in area improvement.

The circuit diagrams and operation principles of 2 T 2FeFETs, 2FeFETs TCAM are as follows. In the 2 T 2FeFETs TCAM, a negative voltage of −2 V is applied to the Bit Line (BL) node to polarize it to High-V_{th} for writing "1", while a voltage of 2 V is applied to the Bit Line Bar (BLB) node to polarize it to low-V_{th} for writing "0". When searching for "0", the Match Line (ML) node is discharged, and vice versa when writing "0" and searching for "1". Additionally, when writing "X" and searching for "0" or "1", the ML node is not discharged, and it operates as a match (Supplementary Fig. 4a–c).

In contrast, the 2FeFETs TCAM performs both search and polarization using Search Line (SL) & Search Line Bar (SLB) (Supplementary Fig. 4d–f). Due to this, when the device is in a low-V_{th} state and the read voltage is below the threshold voltage, the FeFET should be turned off. Therefore, a *I*–*V* hysteresis curve shifted to the right not existing *I*–*V* hysteresis curve, achieved through gate work function engineering (Fig. 8a), is needed. In the high-V_{th} and low-V_{th} states, the FeFET operates as off when the operating voltage is below the threshold voltage, and in the low-V_{th} state, it operates as on when the read voltage is above the threshold voltage.

2FeFETs TCAM has one pull-down transistor, while 2 T 2FeFETs TCAM has two, showing multi-bit mismatch characteristics unlike other TCAM schemes[34]. Figure 8b shows the variation in ML node discharge rate based on the number of mismatch bits in a 64×64 array. The 2FeFETs TCAM, despite its drawback of slower delay, has the advantage of being able to determine the number of mismatch based on the discharge rate.

We investigate and compare the circuit characteristics (Search Delay, Search Energy, and Energy Delay Product) of 16 T, 2 T 2FeFETs, and 2FeFETs TCAM. Additionally, we examine the temperature-dependent

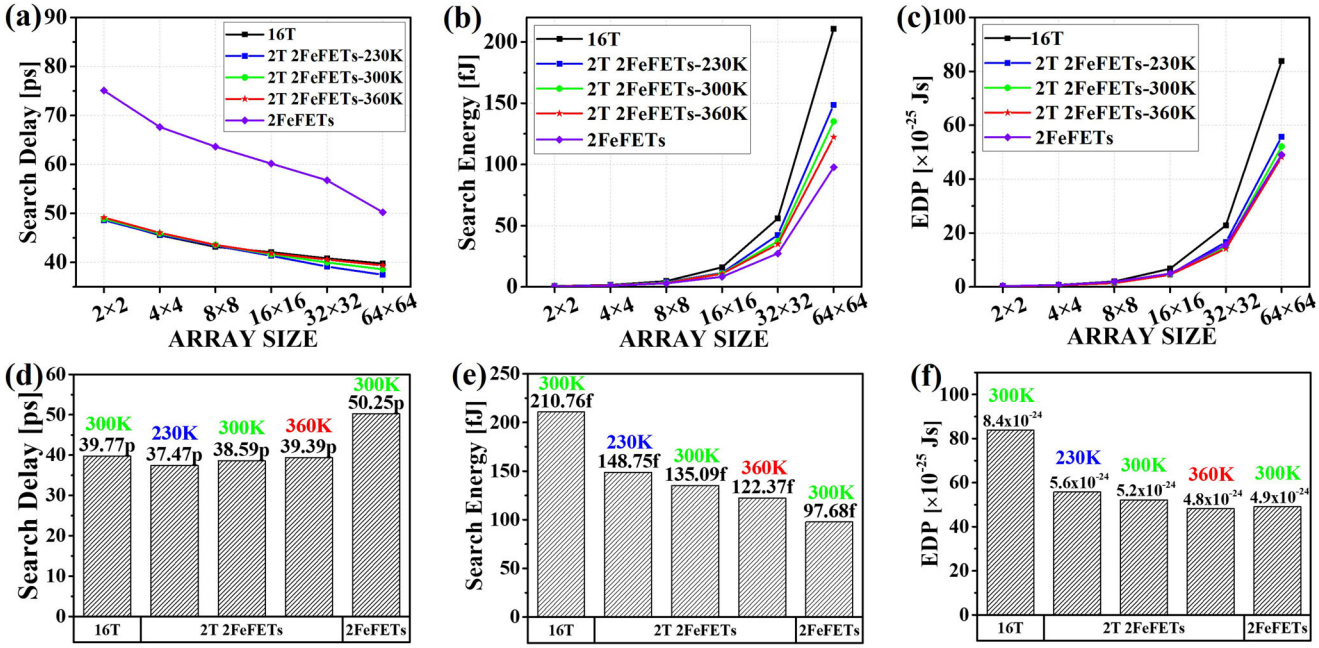


Fig. 9 | Results according to TCAM array size by temperature. **a** Search Delay, **b** Search Energy, **c** EDP, Comparison of (**d**) Search Delay, **e** Search Energy, **f** EDP in 64 × 64.

characteristics of the 2 T 2FeFETs TCAM. To observe trends in performance gaps, we conduct a comparative analysis based on the increase in TCAM array size up to 64×64[35–37].

For comparison between various TCAM schemes, Search Delay, Search Energy, and Energy Delay Product (EDP) are measured in all mismatch states with the highest ML discharge rate of 2FeFETs TCAM. Unlike 1 mismatch, in the case of all mismatches, the number of nodes discharged in the pull-down network increases, leading to a decrease in Delay as the array size increases (Fig. 9a). At room temperature, compared to the 64 × 64 size 16 T TCAM, the 2 T 2FeFETs TCAM is 3.0% faster, while the 2FeFETs TCAM is 26.4% slower (Fig. 9d). The 2 T 2FeFETs TCAM, with two pull-down transistors, exhibits the fastest Delay, followed by the 16 T and 2FeFETs TCAM. For Search Energy, as the transistor count decreases to 1/4 for 2T 2FeFETs TCAM and 1/8 for 2FeFETs TCAM compared to 16 T TCAM, the difference between them increases with the increasing array size (Fig. 9b). Compared to 16 T TCAM, the energy consumption of 2 T 2FeFETs TCAM improved by 35.9%, and for 2FeFETs TCAM, it improved by 53.7% (Fig. 9e). To assess the impact of the trade-off between Delay and Energy, we examined the EDP. In the case of a 64 × 64 size at 300 K, the EDP for 2 T 2FeFETs TCAM is 37.8% lower compared to 16 T TCAM, and 2FeFETs TCAM shows a 41.4% reduction (Fig. 9c, f).

Since the delay of 2 T 2FeFETs TCAM has the largest I_{on}/I_{off} at low temperatures where the on current of FeFET is large and the off current is small, the lower the temperature, the higher the performance. Conversely, Energy consumption has an advantage at higher temperatures when the on current is low.

As a result, 2 T 2FeFETs, 2FeFETs TCAM using FeFETs have an advantage in terms of EDP compared to the 16 T TCAM. This is primarily due to significant energy consumption. In the case of 16 T TCAM, volatile LiM continuously consumes energy in SRAM, while in the 2 T 2FeFETs TCAM, SRAM is replaced by FeFET, reducing energy consumption (Supplementary Fig. 5a). In the 2FeFETs TCAM, the comparator is combined with FeFET, achieving even greater energy savings (Supplementary Fig. 5c).

The 16 T, 2 T 2FeFETs, 2FeFETs TCAM require one Sense Amplifier (SA) per Match line, and each SA consists of three transistors. A 2×2 TCAM cells with SA in the 16 T TCAM have a total of 70 transistors. The 2 T 2FeFETs TCAM has 8 FeFETs and 14 transistors, while the 2FeFETs TCAM has only 8 FeFETs and 6 transistors. Supplementary Figure 3, Supplementary Table 3 compared the layout and area of a 2 × 2 TCAM cell, including SA, for 16 T, 2 T 2FeFETs, 2FeFETs TCAM. The 2 T 2FeFETs TCAM occupies 20.8% less area than the 16 T TCAM, while the 2FeFETs TCAM has a 14% smaller footprint.

Discussion

In this paper, two different types of FA and TCAM were designed through FeFET incorporating ferroelectric materials into 2D-channel DGFETs using monolayer WS_2 channels to confirm the potential for next-generation LiM applications. To achieve this, we examined the structure and characteristics of FeFET and implemented a FeFET compact model. We analyzed the Delay time, Dynamic Power, Standby Power, and Power Delay Product (PDP) for a 28 T FA and 3 FeFETs FA, as well as a 6 FeFETs FA. Additionally, we conducted a circuit layout area comparison through LVS processes applying sub-2nm technology nodes. The same process was carried out for Search Delay, Search Energy, and Energy Delay Product (EDP) aspects in 16 T TCAM, 2 T 2FeFETs TCAM, and 2FeFETs TCAM.

To verify the operational characteristics of the LiM circuit, a FeFET hysteresis curve is essential. If the appropriate Program/Erase voltage is not applied to the gate, a hysteresis loop will not form, leading to operational errors. We optimized the Program/Erase voltage conditions for polarization characteristics, confirming the normal operation of FeFET-based FA and TCAM under various temperature conditions (230 K, 300 K, 360 K).

The PDP of FA improves as the number of utilized FeFETs increases. Compared to 28 T FA, 3FeFETs FA shows a 38.1% improvement, and 6FeFETs FA demonstrates a 64.8% enhancement. The designed 6 FeFETs FA outperforms in terms of Delay time, Dynamic/Standby Power, and PDP under all temperature conditions, with a 13.1% reduction in circuit area compared to 28 T FA, enhancing the feasibility of LiM application circuits. For TCAM, as the array size increases, Search Delay decreases, and the 2 T 2FeFETs TCAM with two pull-down transistors proves to be the fastest. In terms of Search Energy, the 2FeFETs TCAM, with the fewest number of devices among NV TCAM, exhibits significantly the lowest energy consumption. Moreover, examining the temperature characteristics of the 2 T 2FeFETs TCAM reveals that it achieves the fastest delay at the lowest temperature with the highest I_{on}/I_{off}, while energy consumption is most improved at the highest temperature with the smallest I_{on}. Ultimately, at room temperature, the EDP of 2 T 2FeFETs TCAM is 37.8% better than that

of 16 T TCAM, and 2FeFETs TCAM is 41.4% better. Therefore, the EDP of 2FeFETs TCAM is the most superior, with only a 14.0% reduction in area compared to 16 T TCAM.

Methods

Device analysis and circuit modeling of 2D-channel DG FeFET

The temperature characteristics of WS_2 were derived from measurements reported by Ovchinnikov et al.[38], with additional details provided in our research group's previous paper[22]. I_{on} decreases with temperature, while I_{off} increases proportionally to temperature. 2D materials exhibit Metal-Insulator Transition (MIT) characteristics due to the formation of disorder and interactions between metal and insulator, influenced by the relative strength of each mechanism[39]. In monolayer WS_2 DG FETs, MIT occurs at a gate voltage of ~0.3 V, and as the temperature increases, the Sub-threshold Swing becomes higher. When the gate voltage is lower than the MIT point, the influence of the insulating state dominates, resulting in an increase in I_{off} with temperature. Conversely, when the gate voltage is higher than the MIT point, the influence of the metallic state becomes more pronounced, leading to a decrease in I_{on} with increasing temperature[38].

The polarization–electric field (P–E) characteristics of the ferroelectric material used in this study were based on a 10 nm HSO Metal-Ferroelectric-Metal structure measured through PUND tests, with experimental values taken from Ni et al.[30]. Temperature variations were applied based on experimental data reported by Zhou et al.[24]. An increase in the thickness (t_{FE}) of ferroelectrics leads to an enlargement of the MW. However, it also results in an increase in the required voltage for hysteresis, negatively impacting energy efficiency. Moreover, beyond a certain thickness, a monoclinic phase dominates, characterized by minimal remnant polarization and low permittivity, leading to the loss of ferroelectricity[40]. With an increase in temperature, both the MW and Remanent Polarization (P_r) decrease, while the absolute value of Saturation Polarization (P_S) is comparatively small. This is attributed to the phase change in the ferroelectric material; as the temperature of the ferroelectric material increases, the impact of the tetragonal phase with nonpolar characteristics becomes more significant than that of the orthorhombic phase with polar characteristics, resulting in changes in the P–E curve[41].

Data availability

The authors declare that the data supporting the findings of this work are available within the paper and its supplementary information. The corresponding authors can also provide data upon reasonable request.

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Author contributions

H.K. and J.P. contributed equally to the main idea, analyzing the data, and wrote the initial draft of the manuscript. H.J. performed transistor modeling for simulation. J.J. and C.R. planned this research, executed under the supervision, and finalized the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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