

Collaboration, IEDM and 60 years of CMOS



Technology breakthroughs at the 2023 IEEE International Electron Devices Meeting, where collaboration and CMOS technology continue to play their part.

Back in September, the UK rejoined the Horizon Europe research programme¹, resolving an issue that had rumbled on since the UK formally left the European Union (EU) in January 2020. Horizon Europe is the world's largest research-funding scheme. Accessible to member states of the EU and affiliated countries, it has a budget of €95.5 billion and runs until 2027.

As we noted in an Editorial last year², the uncertainty that has surrounded the UK's relationship with Horizon Europe could have long-term consequences for international collaborations in the country. But the UK rejoining the programme was an important step – and a relief to many researchers in the UK. The news of the UK rejoining Horizon Europe has also recently been followed by the announcement that talks on Switzerland rejoining Horizon Europe are set to begin³.

Research thrives on the sort of collaborations that Horizon Europe helps make possible. Such collaborations – whether between researchers from different countries and continents, or from different departments and disciplines – can allow more complex problems to be solved. They can also help more sophisticated technology to be developed.

This is a point that has been repeatedly illustrated by the technology breakthroughs reported at the **IEEE International Electron Devices Meeting (IEDM)**, which takes place in San Francisco in December and has been covered in the journal for the last five years.

We return again to IEDM this year, which is now in its 69th edition, and offer our highlights of the 2023 event.

We begin with work that brings together researchers from the United States and Taiwan – and from across academia and industry – where Ang-Sheng Chou and colleagues report the development of n-type and p-type transistors based on two-dimensional (2D) transition metal dichalcogenides. As Wenjuan Zhu of the University of Illinois at Urbana-Champaign and Xia Hong of the University of Nebraska-Lincoln explain in a **News & Views article**, four key challenges related to creating industrial devices based on 2D materials are addressed in the work: contact resistance, gate dielectric growth, device scaling and integration.

Elsewhere at IEDM 2023, there are developments in device scaling with more conventional materials. Researchers at the Taiwan Semiconductor Manufacturing Company (TSMC) report advances in monolithic complementary field-effect transistors (FETs), where n-type and p-type FETs are vertically stacked. The work, which could lead to improved transistor densities, is discussed in a **News & Views article** from Yeliang Wang of the Beijing Institute of Technology.

Neuromorphic hardware remains an important topic for IEDM. To start, Kerem Camsari and colleagues at the University of California Santa Barbara and Tohoku University report feedforward stochastic neural networks using stochastic magnetic tunnel junctions as probabilistic bits. As noted by Samuel Liu and Jean Anne Incorvia of the University of Texas at Austin in their **News & Views article** about the work, this mixed signal approach has the potential to offer considerable energy savings compared with current digital approaches.

Computing-in-memory (CIM) is another approach that is being used to create

neural network hardware implementations. Jianshi Tang, Haitao Xu and colleagues – who are based at various institutions in China – report a 3D, stackable CIM approach using carbon nanotube transistor and resistive random-access memory arrays. The result is covered in a **News & Views article** by Bokyoung Kim and Hai Li of Duke University.

Sixty years of complementary metal-oxide-semiconductor (CMOS) technology is part of the theme of this year's IEDM, recognizing the anniversary of a report from Frank Wanlass and Chih-Tang Sah at Fairchild Semiconductor on building circuits using complementary n-type and p-type metal-oxide-semiconductor transistors⁴. Inevitably, CMOS technology is central to much of the work at the 2023 event. One example from our highlights is that of Pieter Neutens and colleagues at imec, who report a monolithically integrated platform that combines CMOS electronics and photonic waveguides. The platform is used to create an implantable neural probe for high-resolution optogenetic light excitation and electrical recording. As Aseema Mohanty of Tufts University explains in a **News & Views article** on the work, the approach provides a higher number of recording sites than previous optogenetic neural probes.

The 1963 work on CMOS technology from Wanlass and Sah was not reported at IEDM, but at another long-running meeting in the community: the IEEE International Solid-State Circuits Conference (ISSCC). That meeting now takes place in San Francisco every February, and is another of the events – together with IEDM and the **Symposia on VLSI Technology and Circuits (VLSI)** – that we currently cover in the journal. We will return again to these events in 2024, where the necessity of collaboration will undoubtedly still be on display.

Published online: 21 December 2023

References

1. Sanderson, K. & Naddaf, M. *Nature* **621**, 235–236 (2023).
2. *Nat. Electron.* **5**, 541 (2022).
3. Dixon, E. EU to begin 'exploratory talks' with Swiss on Horizon Europe. *Times Higher Education* (22 November 2023); <https://go.nature.com/46N8IMX>
4. Wanlass, F. M. & Sah, C. T. In 1963 *IEEE Int. Solid-State Circuits Conference Digest of Technical Papers* 32–33 (IEEE, 1963); <https://doi.org/10.1109/ISSCC.1963.1157450>

