REVIEW ARTICLE

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Topological electronics

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Within the broad and deep field of topological materials, there are an ever-increasing number of materials that harbor topological phases. While condensed matter physics continues to probe the exotic physical properties resulting from the existence of topological phases in new materials, there exists a suite of "well-known" topological materials in which the physical properties are well-characterized, such as Bi_2Se_3 and Bi_2Te_3. In this context, it is then appropriate to ask if the unique properties of well-explored topological materials may have a role to play in applications that form the basis of a new paradigm in information processing devices and architectures. To accomplish such a transition from physical novelty to application based material, the potential of topological materials must be disseminated beyond the reach of condensed matter to engender interest in diverse areas such as: electrical engineering, materials science, and applied physics. Accordingly, in this review, we assess the state of current electronic device applications and contemplate the future prospects of topological materials from an applied perspective. More specifically, we will review the application of topological materials to the general areas of electronic and magnetic device technologies with the goal of elucidating the potential utility of well-characterized topological materials in future information processing applications.

To date, the majority of information processing is done using complementary metal oxide semiconductors (CMOSs), an architecture based on a series of interconnected semiconductor devices each performing a different function that aids in the overall goal of processing digital information. The societal demand for smaller-sized electronic devices such as computers and cellular phones with improved functionality has forced not only the sizes of the constituent components of CMOS information processing to rapidly and inexorably shrink but also for the operational frequencies to increase. The required increases in device performance have led traditional semiconductor device technology to reach fundamental, and perhaps ultimately insurmountable, limits of several key quantities, namely, size, weight, and power (SWaP). Specifically in terms of information processing architectures, the most crucial of the SWaP limitations is that of power consumption. In order to continue the march toward ever smaller yet more efficient information processing systems, the architectures have undergone major renovations such as moving to multiple logical core processing in order to circumvent the limitations in power consumption. Yet, the imposition of multicore processing has resulted in a slower rate of improvement than previously demonstrated by increases allotted by transistor scaling[1]. Therefore, finding a methodology to reduce the SWaP of constituent CMOS devices while increasing overall operational efficiency represents an eminent international grand challenge.

While the need to abandon the traditional architectures associated with transistor scaling is generally accepted, the material in which to implement these new architectures is very much an open debate. The requirements for low-power and high-frequency responses have not been satisfied despite many years of intense development. Such realization thereby necessitates the introduction of new classes of materials with correspondingly new physical responses compared to those of traditional semiconducting compounds. One may search for new materials and

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associated excitations by re-examining previously well-understood materials. In doing so, we recall that the discovery and subsequent classification of different phases of matter in terms of the symmetries present, based on the theory by Landau and Lifshitz[2,3], has been at the forefront of condensed matter physics for >70 years. Nevertheless, the theory of phase transitions in condensed matter systems required an extension to include the ideas of topological phase transitions and topological order to account for experimental observations of the integer[4,5] and fractional quantum Hall regime[6]. A topological phase is unique in that it does not break any of the underlying symmetries of the system and cannot be described by a local order parameter[7]. In other words, the inherent properties of the system cannot be changed by adiabatic shifts in materials parameters unless the system passes a quantum critical point associated with a phase transition.

Materials exhibiting topological phases arising from band-structure effects are generally referred to as topological insulators (TIs). Generally speaking, TIs are a class of materials with an insulating time-reversal invariant (TRI) bandstructure for which strong spin–orbit interactions lead to an inversion of the band gap at an odd number of time-reversed points in the Brillouin zone[8–11]. There currently exist a series of known topological materials that meet these criteria, such as HgTe/CdTe quantum wells[12,13] and transition metal dichalcogenides Bi_2Te_3 and Bi_2Se_3[14]. Due to this TRI band inversion, TIs possess very unique properties, such as spin–momentum locking of the surface states[14], magneto-electric effect[15], and lack of backscattering[16]. The TI of most technological relevance is Bi_2Se_3, which has been experimentally shown to be a TI at room temperature with a topologically non-trivial energy gap of 0.35 eV, as observed using angle-resolved photoemission spectroscopy[11,14]. The unique properties of these topological states may also have a significant impact on post-CMOS devices and information processing technologies.

While promising, it remains to be demonstrated that the unique properties of TI may be exploited to enable new device technologies. In this review, we examine the current state of the field in assessing the relevance of TIs in the overall landscape of enabling new electronic and magnetic device technologies within the general overall landscape of both CMOS and beyond-CMOS information processing. More specifically, we will examine the current work in charge transport devices and magnetic devices where each technological implementation is enabled by the unique properties of TIs. Additionally, where possible and appropriate, performance comparisons with other relevant current and next-generation technologies are made so as to quantify the progress that TIs have made and assess their future prospects. We note that, in choosing to focus on the charge and magnetic technologies, we omit mention of the fundamental and important work on TIs for thermoelectric applications. Unquestionably, work on thermoelectric devices falls within the dominion of a review whose stated purpose is to survey the advances in the application of well-characterized TIs for future device technologies, and there exist several excellent reviews of topological thermoelectrics that we recommend to the interested reader without reproducing their work[17–20].

Topological electronic devices
We begin the survey with a review of the most salient work performed toward using topological materials as the foundation for new types of nanotechnology by examining charge transport in TI as it pertains to relevant CMOS applications. More precisely, we will examine charge transport in active device structures with the purpose of developing (1) new transistor technologies

and (2) new local electrical interconnects, again as examined within the limited scope of currently available topological materials rather than those materials that are not yet sufficiently characterized, in which case questions about device applicability are either premature, or the materials that are not broadly available, or both.

Topological field-effect transistors (FETs). Given a new material, such as a TI, an obvious application is that of the essential building block underlying all CMOS architectures, the transistor. At first glance, the properties of TIs, and more specifically, Bi_2Se_3, may lend themselves quite naturally to function effectively as a transistor material due to the inherent lack of backscattering in the topologically protected surface states. Therefore, charge transport within the protected surface state has the benefit of being immune to the charged impurity scattering that may deeply affect the properties of nanoscale MOSFETs. Nonetheless, the presence of a metallic surface state raises the immediate question as to how an applied electric field will be able to tune the carrier densities of the TI. Within this context, the path to the realization of a TI transistor begins with the earliest attempts to examine FET structures using Bi_2Se_3 as the channel material. The initial studies utilized cleaved bulk Bi_2Se_3 films of thickness ≈100 nm in dual gate configuration where there is a back gate and a top gate that may be used to independently tune the carrier densities[21,22]. The fabricated devices show evidence of three parallel conductive channels resulting from the two surface states and the populated bulk states. However, despite the presence of significant bulk carriers, electric field gating is capable of altering the dominant carrier type from electrons to holes, which is a fundamental prerequisite for eventual CMOS implementation[22].

An obvious problem arises due to the presence of 10^{18}–10^{19} cm^{-3} bulk states resulting from the effects of unintentional selenium vacancy doping[22–24]. The presence of such states is deleterious to FET operation as it provides a less resistive path for current flow as compared to the higher resistance two-dimensional (2D) topological surface states. Therefore, in such a situation, one would expect that the majority of the current would be shunted through the ample bulk states inhibiting the observation of benefits resulting from conduction via the topological surface states. A potential route to minimize the contribution of the trivial bulk electrons is to utilize the confinement of thin TI samples for FET devices. FETs consisting of ultra-thin (thickness 3–14 nm) exfoliated Bi_2Se_3 on 300 nm SiO_2/Si substrates that also function as the gate electrode[24]. In Fig. 1a, we display measured plots of the conductance of a 3.5-nm-thick Bi_2Se_3 FET at a variety of different temperatures. While the FET did not produce evidence of drain current saturation or ambipolar conduction characteristic of traditional semiconductor FETs, the transport measurements confirm that, with sufficient gate voltage, the thin-film Bi_2Se_3 may be depleted of electrons, both on the surface and in the bulk, to form an insulator.

It is clear that reducing the thickness of the TI films to reduce the bulk conductivity allows for subsequent electrostatic gating that is capable of removing much of the bulk doping without inducing breakdown. Therefore, the simple production of cleaved thin-film TI samples is sufficient to produce the "off" state that results from the complete depletion of bulk doping. Unfortunately, reduced sample size alone is insufficient to be able to change the dominant doping from n-type to p-type in thin-film TI samples[24]. In an effort to shift the chemical potential further toward the edge of the conduction band edge, improvements to TI-FET devices examined the incorporation Ca dopants that substitute for the Bi atoms into Bi_2Se_3 crystals[25]. For ultra-thin FET geometries, the addition of Ca atoms to the material reduces the bulk carrier concentration so that electrostatic gating switches n-type behavior
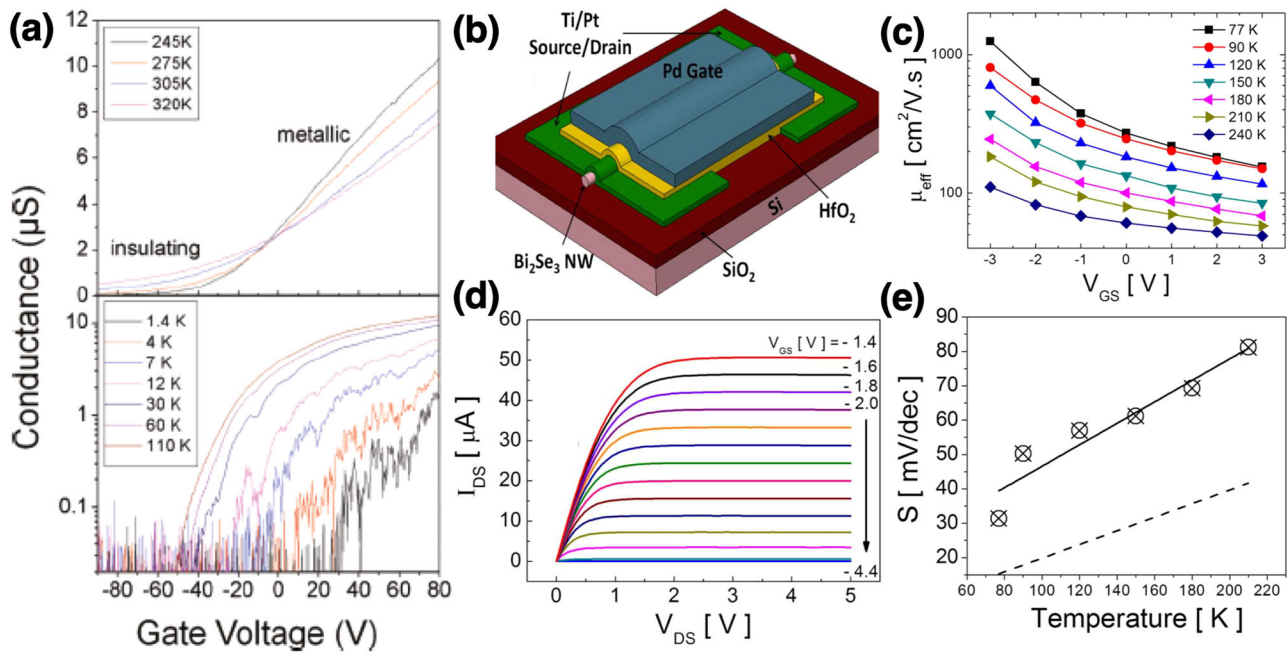
Fig. 1 Topological transistors. a Experimental measurements of the conductance versus the applied gate voltage showing metallic and insulating behavior of ultra-thin 3D topological insulator Bi_2Se_3 FETs at a variety of different temperatures. Reprinted (adapted) with permission from ref. [24], copyright 2011. **b** Schematic illustration of the design of a gate-all-around (GAA) design of a nanowire FET fabricated in Bi_2Se_3[29]. **c** The thermal evolution of the experimentally extracted effective mobility within the channel of the Bi_2Se_3 nanowire FET as a function of the applied gate voltage[29]. We immediately notice that the mobility is far less than typical semiconductors currently used in CMOS devices. **d** The drain terminal current, I_{DS}, plotted against the applied drain voltage, V_{DS}, at $T_{sys} = 77$ K demonstrating that typical transistor transfer curves may be obtained in topological FETs[29]. **e** The sub-threshold slope as extracted from nanowire topological FETs (solid line) showing that the incarnation of the topological FET requires more energy to switch from the "off" state to the "on" state than an ideal FET. Reprinted by permission from ref. [29], copyright 2013.

to p-type. The Ca-doped samples still exhibit parallel conduction through bulk and surface states, nonetheless the bulk conductivity is smaller than the surface contribution up to temperatures of $T_{sys} = 130$ K[25]. Additionally, one may be concerned about the formation of a bulk impurity band within the TI bulk band gap resulting from the addition of high dopant concentrations. Yet, the possibility of an induced bulk impurity band is excluded as a potential factor that may occlude the observation of surface state conduction due to the fact that bulk impurity bands are normally populated by carriers that are of lower carrier mobility than the measured bulk mobility. In a similar manner, thin-film FET behavior is observed in films grown by molecular beam epitaxy (MBE) where surface state conductivity dominates for film thicknesses from 2 to 256 nm for $T_{sys} < 30$ K indicating that not only sample preparation but also sample growth conditions play a role in the resultant transfer characteristics[26]. While the thin-film geometry offers a simple path to the reduction of the deleterious bulk states, within the TRI topological materials we consider in this review, there is a clear limit to the reduction in thickness possible. Experiments have clearly demonstrated that when the thickness of three-dimensional (3D) topological materials is reduced below 5 quintuple layers (QLs), where one QL is 0.955 nm in thickness. Below these thicknesses, there is an appreciable intersurface tunneling between the normally isolated surfaces that leads to the formation of a gap in the energy spectrum[27]. Yet, there is theoretical work that points to the fact that the gapped thin-film TIs have distinct properties from the thicker materials such as a vanishing in-plane spin component and Berry curvature close to the gap edge in momentum space. Exploiting these new properties, should they be experimentally accessible, may lead to new applicability of thin-film TIs once they are more clearly understood[28].

The culmination of early examinations of topological FETs focuses on utilizing design that is closely connected to current CMOS transistors by utilizing Bi_2Se_3 nanowires in the gate-all-around (GAA) configuration, shown schematically in Fig. 1b. The International Roadmap for Devices and Systems (IRDS) predicts that the GAA transistor design will be in use in nanoscale FETs by 2024[1]. In the GAA configuration, single-crystal Bi_2Se_3 nanowires of various sizes ranging from 50 to 150 nm wide with a corresponding length of 10 μm are surrounded by a HfO_2 gate dielectric and subsequently covered by a Pd gate metal[29]. The source and drain contacts are Ti/Pt and the entire structure is built upon a SiO_2/Si layer beneath the FET. Subsequent electrical characterization of the FET is performed at $T_{sys} = 77$ K. The TI nanowire FET shows similar unipolar conduction dominated by electrons, as one may expect from Se vacancy doping[23,24], and an excellent I_{on}/I_{off} ratio that exceeds 10^8, albeit at a temperature that is far lower than room temperature. In Fig. 1c, we show the I_{DS}–V_{DS} curves that show behavior similar to the cutoff, linear, and saturation regimes of a semiconductor MOSFET; however, the saturation regime in the I_{DS}–V_{DS} curves occurs not due to pinch-off of the nanowire at the drain end of the FET, as is the case in a conventional MOSFET, but due to velocity saturation at the source end of the FET. Nonetheless, recent improvements in crystal growth techniques have seen the fabrication of p–n junctions in Bi_2Se_3 that allow for ambipolar conduction with physics identical in form to conventional semiconductor FET electrostatics, but it is unclear as to how such as process takes advantage of any unique topological characteristics[30].

The I_{DS}–V_{DS} curves produced by the GAA topological FET are encouraging in that the results demonstrate that TIs may potentially be used as effective channel replacement materials in future CMOS applications. Yet, there are two important measures

that have not been addressed in the examination of the topological FET: carrier mobility within the transistor and the sub-threshold slope. In Fig. 1d, the effective carrier mobility, extracted from the linear portion of the $I_{DS}-V_{DS}$ curve in Fig. 1c, is plotted for a variety of different gate voltages at temperatures ranging from $T_{sys} = 77$ K to $T_{sys} = 240$ K. At $T_{sys} = 77$ K, the electron mobility in the transistor is $\mu_{eff} = 1300$ cm^2/V·s but decreases appreciably to $\mu_{eff} = 100$ cm^2/V·s as the temperature approaches room temperature, which is both indicative of both the dominance of phonon scattering in setting the value of the mobility and the significantly reduced value as compared to silicon nanowires of the same dimensionality at room temperature[1]. Additionally, one of the most important figures of merit for a transistor implementation is the sub-threshold swing, S, or the change in gate voltage required to change the current by one order of magnitude. In Fig. 1f, the sub-threshold swing of the topological transistor is plotted as a function of temperature. One quickly observes that the value of S for the topological transistor is significantly greater than that of the ideal transistor at the same temperature. Taken in tandem, Fig. 1d, e demonstrate that, for the topological FET to compete with current CMOS technology or band–band tunneling transistors[31,32], there are many materials and fabrication issues that are yet to be solved, if possible.

Corresponding theoretical work on the overall relevance of TI for FET applications has, to this point, rendered inconclusive results as to the eventual benefit derived from utilizing TI in transistor applications. The results suggest that ultra-thin TI films, in which the top and bottom surface states interact to open a gap, may either provide an excellent material for FET implementations[33] or one that may be fundamentally plagued by short channel effects due to the high relative dielectric constant of Bi$_2$Se$_3$ which is $\epsilon_r \approx 100$[34]. Theoretical examinations of both 2D[35–37] and 3D TI[33,34,38–40] for transistor applications have examined various different types of device implementations that show promise in being able to meet IRDS standards for SWaP characteristics in certain categories. Yet, when the device characteristics are taken in aggregate, they do not appear to be competitive with other more traditional semiconductor nano-transistor implementations. The types of physical effects that have been theoretically explored in this search span a virtual cornucopia. Within 2D TI, these methods include gate-modulated backscattering in 2D HgTe nanoribbons[36], gate-induced energy gap modulation by coupling of the edge states to electrostatically induced channels[37], and electric field-induced topological to trivial phase transitions in transition metal dichalcogenides[35] and crystalline insulators[39]. In 3D theoretical studies, the mechanisms include traditional FET implementations[33,34], piezoelectric modulation of the strain in 3D TIs[40], and both electric field-induced[38] and piezoelectric strain-induced topological phase transitions[41].

Having discussed many of the significant steps within the experimental and theoretical exploration of topological materials in the service of creating new active information processing device technologies, it is worthwhile to examine how the performance of these devices compares to other current technologies. In making this comparison, we utilize the established methodology codified for benchmarking disparate technologies[36,42,43] to determine the switching delay as a function of the intrinsic switching energy associated with each switching event. By calculating the switching energy per operation for disparate technologies, we may properly assess the degree to which topological materials may improve technologies over current and proposed solutions. In this comparison, we use both theoretical[36] and experimental[29] data on the performance of topological transistors and compare it with the performance of
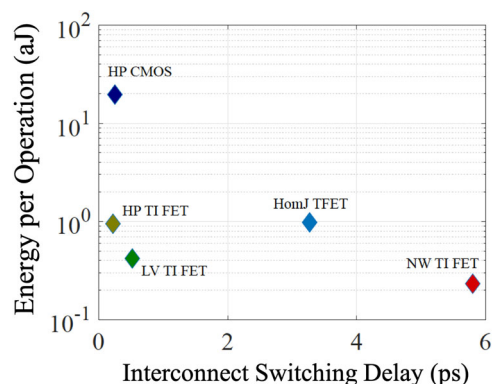

Fig. 2 Benchmarking topological field effect transistors. Comparison of the experimental (TIFET) and theoretical low-voltage (LV) and high-performance (HP) approaches[36] to the design of a FET based on the use of topological materials with other established competing FET technologies, such as the homojunction tunnel FET (homJTFET) and current high-performance CMOS technologies (HP CMOS). The comparison is based on the amount of energy that is dissipated per operation for each technology plotted against the interconnect delay in current CMOS technology. The approach utilized here follows the methodology in refs. [42,43]. We conclude that, while there are many areas that may be improved to increase the performance of topological materials in FET technologies, they are not currently a competitive alternative to CMOS. Nonetheless, theoretical estimates demonstrate that topological transistors have sufficient promise to offer marked increases in performance at reduced power consumption when compared to current FET technologies.

homojunction tunneling FETs and current high-performance CMOS technologies[43]. Within Fig. 2, the results of the comparison illustrate that, of all the technologies considered, the high-performance CMOS transistors consume the most energy; however, they are capable of switching quickly thus making them extremely competitive with the other technological solutions. The theoretical estimates indicate that topological FETs (TIFET LV and HP)[36], with appropriate improvements, may be capable of competing with current CMOS technologies as there are potential advantages in both energy usage and intrinsic switching delay that exceed an order of magnitude improvement over the state-of-the-art CMOS. Nevertheless, the current incarnations of topological FETs are plagued by large capacitances and are, thus, incapable of being a competitive technology when compared with other current FET technologies. Yet, even in the unoptimized incarnation illustrated in Fig. 2, we observe an order of magnitude reduction in the energy usage in topological FETs. Currently, the potential technological advantages that TIs possess, in the form of protection from backscattering, do not seemingly provide a route that will result in significant improvement in either mobility or drive current when compared to current CMOS technologies. In this light, to be a viable future FET technology, additional electrostatic control and reduced parasitics are required to allow them to be considered as competition for implementation in future information processing technologies.

Topological p–n junctions. In traditional semiconductor formulations of transistors, the underlying operational principles are based on the fabrication and manipulation of successive p–n junctions. In the context of TIs, however, the concept of the p–n junction is not expected to be a system that produces the simple injection of charge carriers modulated by the electric field manipulation of the built-in potential between the electron-doped n-side and the hole-doped p-side. Theoretical studies of
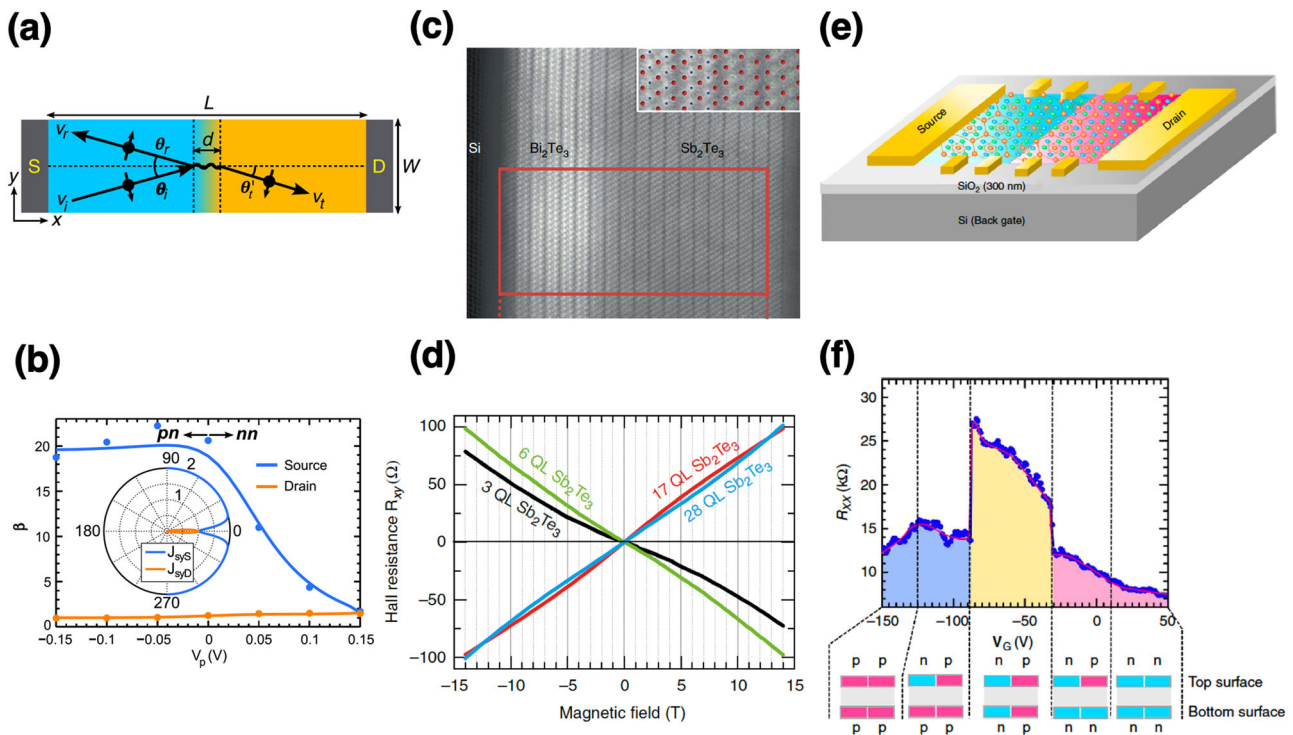
Fig. 3 Topological p–n junctions. a Theoretical schematic illustrating the surface of a 3D TI p–n junction with incident, reflected, and transmitted electrons shown with their corresponding spin polarizations. Image taken from ref. [47]. **b** Calculated quantum transport results showing the spin-to-charge ratio, β, at the source and drain contacts as a function of the gate voltage V_p applied to the p-type part of the junction at a fixed gate voltage on the n-type part of the junction. We observe a large enhancement in β at the source contact in a topological p–n junction due to the spin-momentum locking of the surface states of a 3D TI. Image taken from ref. [47]. The inset shows that the transmitted current is only non-zero when the incident electrons are normal to the surface of the junction. **c** A high-angular annular dark field image of two MBE-grown binary 3D TIs, 15 QL of Sb_2Te_3, and 6 QL of Bi_2Te_3 in direct contact with one another. Image taken from ref. [49]. **d** Experimentally measured Hall resistance of various heterostructures comprised of 6 QL of Bi_2Te_3 with differing Sb_2Te_3 thicknesses. Image taken from ref. [49]. **e** Schematic of a horizontal p–n junction with a Si back gate to tune the location of the chemical potential. On one half of the surface, an electronegative molecule is deposited on the surface to draw out the unintentional bulk carriers allowing greater manipulation of the chemical potential with electrostatic gating[48]. **f** Quantum transport measurements of the longitudinal resistance of topological p–n junction as a function of back-gate voltage V_G showing a large jump in resistance when there are p–n junctions formed on both the top and bottom surfaces. The jump in resistance is attributed to the spin-momentum locking of the surface states in a 3D TI[48].

topological p–n junctions have revealed that the interference between incident waves impinging on the p-side from the n-side results in an experimentally observed standing wave pattern on the surface with power–law decay[44]. When placed in a magnetic field, the topological p–n junction possesses a chiral edge state at the interface between the two differently doped regions[45]. Yet, the resultant chiral edge state may be thought of in more general term as a the state that appears at the interface between two different regions of local Hall conductance[46]. Using this more general understanding of the chiral edge state, selective electrostatic gating may create different regions of n-type and p-type doping on the top and bottom surfaces that, in conjunction with the inherent spin–momentum locking of the surface states in a 3D TI, serve to form a spin-dependent Mach–Zender interferometer.

Each of the aforementioned applications of p–n junctions within TI does not hold promise to be useful as the operational basis for a future electronic device. The production of edge states in topological p–n junctions requires the presence of a large magnetic field and correspondingly low operational temperatures. More recent theoretical and experimental progress has, however, revealed that usefulness of the p–n may reach beyond low temperatures. Consider in Fig. 3a the familiar p–n junction configuration on the surface of a TI connected to source and drain contacts. Electrons are injected from the n-type side to the p-type side at a range of angles relative to the interface normal to the p-type side. Analogous to electromagnetic waves impinging

on a surface, the incident electrons are separated into reflected and transmitted components after the interaction with the barrier. The nature of the transmitted and reflected electrons are different on the surface of a TI due to the presence of the strong spin–orbit coupling and the associated spin–momentum locking[47]. As electrons move under bias from the source contact to the drain, they undergo scattering if they arrive at an angle deviated from normal incidence at the interface. Thus, only electrons arriving normal to the p–n junction interface are transmitted while all other angles are reflected. The scattering at the p–n junction interface causes a change in the momentum and with it the associated spin angular momentum. The resultant reflected wave is then comprised of a spin angular momentum that has flipped from its original incident direction and the transmitted wave that has the same spin component as the original incident electron wave. Accordingly, the result of the filtering of the transmitted and reflected waves is an enhanced ratio between the spin current components while, at the same time, decreasing the transmitted charge current. In Fig. 3b, we plot the results of theoretical calculations corresponding to the ratio between the spin and charge currents at the source contact, β_s, and drain contact, β_d, of a horizontal p–n junction on the surface of a 3D TI when the gate voltage on the n-type side is set to $V_n = 0.15$ V while the p-type gate potential, V_P is varied. We observe a large value of β_s when there is a well-developed p–n junction and spin filtering occurs at the interface attaining a value
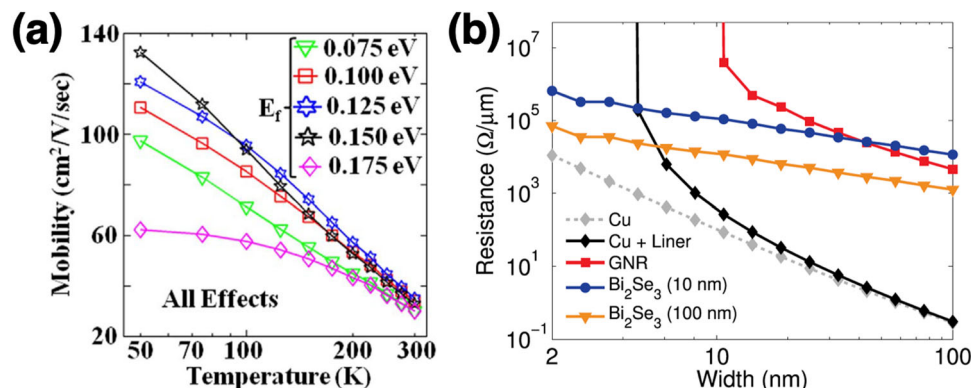
Fig. 4 Topological interconnects. a Numerically calculated mobility of electrons in Bi_2Se_3 nanowire interconnects when considering non-ideal effects, such as roughness scattering and phonons, as a function of the simulation temperature for various Fermi levels[59]. Reprinted by permission from ref. [59], copyright 2014. **b** Theoretical resistance, normalized by the length, of different interconnect technologies compared to that of Bi_2Se_3 nanowire interconnects as calculated for two different mean-free paths of 10 nm (blue) and 100 nm (orange)[60].

of close to β_s 20 at the source contact while it remains close to β_d 1 at the drain contact, where one does not expect spin–charge separation due to the topological surface state. As V_p is modulated from strongly p-type to n-type, the value of β_s becomes equivalent to β_d reflecting the lack of spin filtering in the current as the junction interface gradually becomes more transparent with increasing V_p.

The theoretical work on topological p–n junctions is compelling as a means of providing spin–charge separated currents using the inherent properties of the 3D TI; however, the theoretical picture does not include complications such as charge and spin relaxation that may serve to limit the operational efficiency and temperature. In order to resolve operational questions concerning the topological p–n junction, experimental studies have been performed[48–50] under a variety of conditions. As one may expect, fabrication of topological p–n junctions presents a formidable challenge due to the inherent n-type doping typically observed in 3D TIs[22–24]. In order to surmount the unintentional doping within a TI, there are two main methodologies: growth-based approaches and chemical approaches. Figure 3c presents a high-angular annular dark field image of two MBE-grown binary 3D TIs, 15 QL of Sb_2Te_3 and 6 QL of Bi_2Te_3. The purpose of growing the two TIs in contact with one another is to use charge compensation between the n-type Bi_2Te_3 and the p-type Sb_2Te_3 to alter the position of the chemical potential as a function of position within the heterostructure. In Fig. 3d, we show the transport measurements of the Hall resistance at $T_{sys} = 1.4$ K in heterostructures consisting of 6 QL of Bi_2Te_3 and various thicknesses of Sb_2Te_3[49]. As anticipated, for thin films of Sb_2Te_3 on Bi_2Te_3 the predominant character of the carriers is n-type; however, as the thickness of the films increases the sign to reveal dominant hole transport due to charge compensation between the two TIs.

In opposition to the high-precision interfaces created using MBE, one may use the previously mentioned chemical technique[24] on a single 3D TI to create horizontal topological p–n junctions[48]. In Fig. 3e, we show a schematic of the fabrication of an in-plane topological p–n junction in $Bi_{2-x}Sb_xTe_{3-y}Se_y$ with a Si back gate that can be used to tune the location of the chemical potential of the overall structure. By placing a chemical gel on the surface of part of the junction, the electronegativity of the gel draws electrons from the bulk of the TI allowing for greater tunability of the chemical potential. Using this approach, in Fig. 3f, we plot the experimentally measured longitudinal resistance curves at a temperature of $T_{sys} = 2$ K as a function of the back-gate voltage, V_G. As V_G is modulated from $V_G = 0$ V to

increasingly negative voltages, the dominant carrier type of the bare and chemically treated surface regions changes at different voltages on both the top and bottom surfaces. With increasingly negative V_G, a p–n junction is formed on the top surface accompanied by an increase in resistance. When sufficient V_G is applied to change the carrier type from n-type to p-type on both surfaces, a marked jump in the longitudinal resistance is observed commensurate with the chiral tunneling predicted theoretically[47]. In regions of V_G in which topological p–n junctions are not formed on the two surfaces, the significant jump in resistance is not observed providing further evidence of chiral tunneling being the dominant effect observed. Therefore, while the base temperature utilized in Fig. 3f is too low to resolve the ultimate questions surrounding valid operational regimes for the topological p-n junction, the results do provide an excellent proof of concept that is clearly worthy of additional theoretical and experimental exploration to determine the ultimate utility of these topological devices in the design of new electronic components.

Local electrical topological interconnects. Beyond the need for alternative transistors with reduced SWaP, there are other charge-based active device components that must be reconsidered as technology generations continue to advance. One of the most under-examined of these components is the interconnect that forms the backbone of CMOS packaging. Copper interconnects, while an effective solution for near-term implementations in CMOS packaging applications, suffer from finite size effects that increase the resistivity dramatically and effectively limit their feasibility in future packaging technologies[51]. Specifically, the finite size effects, such as line-edge roughness and grain-boundary scattering, are predicted to raise the resistivity of copper to levels unfit for usage as interconnects[52]. The change in resistivity within copper nanowires increases both the dissipation and the signal delay when copper is reduced to nanoscale sizes[53]. Such increased resistivity is predicted to result in the "interconnect bottleneck" in which the poor performance of the nanoscale interconnects is the limiting factor in the continuous scaling of CMOS technologies[54].

In seeking to overcome the "interconnect bottleneck," other solutions have been proposed to supplant copper as the dominant interconnect material. For example, zigzag graphene nanoribbons have been proposed due to their high mobility carriers[55]. However, the use of graphene nanoribbons is fraught with difficulties yet to be surmounted. To be more specific, graphene nanoribbons suffer from growth and processing-induced defects and line-edge roughness that limits the value of the mobility in nanoribbons[56,57]. Furthermore, graphene nanoribbons are well
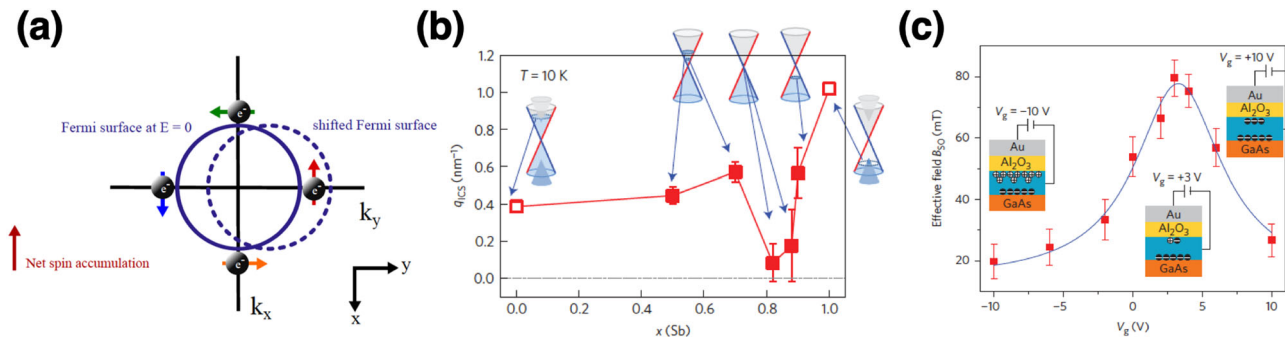
Fig. 5 Topological spin–orbit torque (SOT). a Schematic of the physics behind the SOT, namely, when an electric field is applied to a topological insulator, the shift of the Fermi surface causes an imbalance in spins allowing a spin Hall current to develop perpendicular to the charge current flow on the surface[71]. Reprinted by permission from ref. [71], copyright 2014. **b** Experimentally obtained value of the spin Hall angle, or q_{ics} here, as a function of the position of the Fermi level demonstrating the importance of tuning the Fermi level in a topological SOT device[72]. Reprinted by permission from ref. [72], copyright 2016. **c** Plot of the value of the spin Hall angle as modulated by an applied electric field in a magnetic topological insulator[73]. Reprinted by permission from ref. [73], copyright 2016.

known to develop a band gap in the excitation spectrum that serves to additionally reduce the conductance[58]. As an alternative to both graphene and copper, the lack of backscattering in TIs that drove the transistor work also has potential for applications as local electrical interconnects in CMOS packaging technologies. In initial theoretical work on the utility of TI films for interconnects, quantum transport theory is applied to TI nanoribbons of thickness between 10 and 13 nm in the presence of acoustic phonons, line-edge roughness, vacancies, and charged impurities[59]. Using this theoretical analysis, Fig. 4a shows the results which illustrate that Bi_2Se_3 nanoribbons suffer from a significantly degraded mobility at room temperature due to the presence of the electron–phonon interaction that effects not only the surface states but also the mobility of the bulk states, particularly as the Fermi level moves higher into the non-topological bulk bands of the material[59]. While this result is theoretical in nature, upon reflection, it is not a surprising result given the results in Fig. 1c. Naturally, one may choose to operate the interconnect within the topological regime where only the surface states are populated as a means to fully utilize the topological nature of the surface states and, again, attempt to exploit the resultant increases in the mobility. While such a strategy does increase the mobility of the surface electrons, the low density of states in the surface state cannot compete with the much higher density of states available in copper interconnects of the same dimensions[59].

Despite the initial negative indications of low mobility and low density of states in TI nanoribbons, further theoretical work on the utility of topological interconnects has revealed that there may yet be a role for TI in future local electrical interconnects[60]. By combining semiclassical and quantum mechanical approaches, a more complete picture of the performance of TI interconnects may be uncovered. In Fig. 4b, we plot various different types of proposed or realized interconnect technologies in which the resistance per unit length is plotted as a function of the width of the interconnect. Despite the ever shrinking widths of the technologies, it is still possible to make performance estimates using semi-classical approaches, such as Matthiessen's rule, due to the fact that the lengths of the interconnects are typically longer than the mean-free path within any given material[61]. For the more specific context of the mean-free path within TIs, theoretical calculations have shown that the immunity from localization does not indicate that 3D TIs possess reduced resistive scattering that may indicate a large mean-free path[62]. In fact, experimental work has elucidated the mean-free path for 28-nm-thick nanoribbons of Bi_2Se_3 at a temperature of 4.2 K at

electron densities in the range of 10^{19} cm^{-3} to be $\lambda_{bulk} = 21$ nm while the mean-free path of the surface is only $\lambda_{bulk} = 28$ nm. The short mean-free paths in 3D TI found at low temperatures convincingly implies that one should not expect the mean-free path to approach the length of the interconnects[63]. The calculations in Fig. 4b are performed using Matthiessen's rule for both Bi_2Se_3 and graphene nanoribbons, whereas the calculations for the copper resistance use a combination of Fuchs–Sondheimer[64] and Mayadas–Shatzkes[65] models for wires of aspect ratio 2, so as to accurately capture the role of sidewall and grain-boundary scattering. The main result contained within Fig. 4b is that the low resistance of copper makes it an ideal interconnect down to nanoscale dimensions of 6 nm even in the presence of the 2 nm diffusion liner that is required by the processing. Below 6 nm, copper interconnects have a rapidly increasing resistance due to increased surface scattering and, it is within this regime, that topological interconnects may be an attractive alternative[60]. Nevertheless, as is the case with the FET implementation, the benefits afforded by TI in interconnect implementations do not make a strong case that they may replace more traditional materials in future interconnect technologies.

Topological magnetic devices
Broadly speaking, much of the work we have summarized in the exploration of TIs for application in electronic technology relies upon the attempted exploitation of the lack of backscattering in TRI TIs. In this regard, the prevailing belief is that the topological protection of the surface states would lead to a high-mobility material that, in turn, would lead to a high-performance FET. Thus far, the potential of TIs in electronic devices has not been clearly realized. In light of this, we now shift our attention to discuss efforts to exploit several other unique properties of TI, namely, the spin–momentum locking of the surface states and the magneto-electric effect in TRI TI. The corresponding efforts to exploit each of these may once again be broadly divided into categories, and while a plethora of magnetic device technologies have been proposed, here we focus on two promising technological applications: (1) spin–orbit torque (SOT) devices for magnetic memory technologies that exploit the spin–momentum locking of the topological surface states and (2) passive device technologies that exploit the magneto-electric effect.

SOT-based topological device technologies. Spin-transfer torques (STTs) are the main physical principle that underpins the operation of magnetic random access memory (MRAM). MRAM is a low-power, non-volatile memory application that uses STT to

perform the *read/write* operation by injecting spin-polarized carriers from a reference layer into a connected recording layer so as to change the orientation of the magnetic moment in the recording layer. The nature of the spin–momentum locking, in which the spin is always perpendicular to the momentum along the Fermi surface, within TRI TI, therefore, offers an opportunity to utilize the strong spin–orbit interaction to generate a large spin Hall current using unpolarized carrier injection. The resulting spin Hall current would then perform the same function as STT in that the interaction of spin-polarized currents alters the orientation of magnetic layers and has been referred to as SOT. The main principle of behind SOT is shown in Fig. 5a where we observe that the application of an in-plane electric field naturally generates a shift in the spin–momentum-locked Fermi surface creating a spin imbalance. The spin imbalance naturally leads to a diffusion of spin that flows on the surface of the TI, or a spin Hall current, without the need for ferromagnetic contacts to inject spin-polarized carriers[66,67].

Studies of the SOT in TI center around detection of spin Hall current generated by injected carriers. The connection between the spin Hall current in the injected carrier current may be defined as $I_{SH} = (h/4\pi e)(L_{ML}/t_{ML})\theta_{SH}I_{CH}$, in which L_{ML} is the size of the magnetic layer, t_{ML} is the thickness of the magnetic layer, and I_{CH} is the injected charge current. Using this definition, the spin to charge conversion ability may be parametrized by the spin Hall angle, θ_{SH}, which, if greater than unity, may represent a material of significant promise for use in future magnetic device technologies. Initial measurements of θ_{SH} in TI indicated small values that show variability depending on both the fabrication and materials growth methodology. Specifically, early measurements of θ_{SH} resulted in values of 0.16 using MBE-grown Bi_2Se_3 of thicknesses between 11 and 45 nm at $T_{sys} = 8$ K[68], 0.15 for $Bi_{1.5}Sb_{0.5}Te_{1.7}Se_{1.3}$ grown by the Bridgeman method that are on the order of millimeters thick measured at $T_{sys} = 15$ K[69], 0.36 for exfoliated Bi_2Se_3 of thicknesses between 15 and 100 nm with data taken at $T_{sys} = 300$ K[70]. Interestingly, in contrast to the relatively small values of θ_{SH} reported, contemporaneous measurements of 8-nm-thick MBE-grown Bi_2Se_3 measured at $T_{sys} = 300$ K exhibited anomalously large values of $\theta_{SH} \approx 2$–3.5[71].

Yet, in each of the aforementioned measurements of the SOT via θ_{SH}, the Fermi level is well within the conduction band of each system, and one expects improvements as the quality of the samples increases and the concentration of bulk carriers is reduced. More recent experiments measuring θ_{SH} in 8 nm (Bi, Sb)$_2$Te$_3$, known to have fewer bulk conductance channels, have shown that the value of θ_{SH} improves 2.5x to 0.4 thereby suggesting that, indeed, the presence of bulk carriers degrades the SOT in topological materials. Subsequently, magnetron-sputtered polycrystalline $Bi_xSe_{(1-x)}$ thin films within $Bi_xSe_{(1-x)}/Co_{20}Fe_{60}B_{20}$ heterostructures, which also have strong quantum confinement, show θ_{SH} as large as 18.6 at room temperature. Clearly, there is a dependence on the position of the Fermi level and the value of θ_{SH} in the TI, and this dependence is clearly elucidated in Fig. 5b where θ_{SH}, here referred to as q_{ics}, as a function of the fraction of Sb doping in 8-nm-thick $Bi_{1-x}Sb_xTe_3$ films at $T_{sys} = 300$ K[72]. As the Sb fraction increases, the Fermi level moves from the conduction band to the valence band. We notice that, as the Fermi level approaches the charge neutral point, the value of q_{ics} decreases appreciably prior to increasing again when the Fermi level moves past the Dirac point illustrating the need to finely tune the position of the Fermi level in order to maximize the SOT possible within a given topological material. To this point, Fig. 5c shows that, by utilizing magnetic topological materials, such as 7-nm-thick $(Cr_{0.16}Bi_{0.50}Sb_{0.42})_2Te_3$, the magnitude of the SOT may be manipulated by a factor of 4× via the application of an applied electric field reaching a maximum value of $\theta_{SH} \approx 0.4$
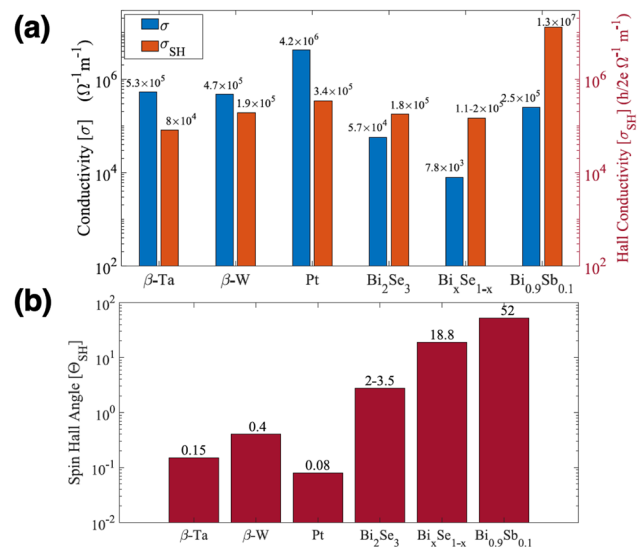

Fig. 6 Benchmarking SOT materials. a Conductivity (σ) and spin Hall conductivity (σ_{SH}) and **b** the resultant spin Hall angle θ_{SH} for several prominent strongly spin–orbit coupled metals (β-Ta, β-W, and Pt) shown in conjunction with common TI materials. While TIs are not as conductive as the metals, due to their comparatively large band gap, they may produce spin Hall conductivities that exceed those of metals. The significant improvement that TIs offer in spin to charge efficiency is captured in the spin Hall angle where it may be as much as two orders of magnitude larger than comparable metals. Both figures are adapted from ref. [74]. Reprinted by permission from ref. [74], copyright 2018.

although the measurement must be done at $T_{sys} = 1.9$ K so as to keep the magnetic system below the Curie temperature[73].

Taken in totality, these values are quite encouraging as they are better than or competitive with other spin–orbit coupled metals, such as Pt, β-W, and β-Ta. As the quality of topological materials and understanding of underlying physics of the SOT improves, undoubtedly θ_{SH} will continue to increase. Much to this point, $\theta_{SH} \approx 52$ has been measured in $Bi_{0.9}Sb_{0.1}$ films <25 nm thick, while, due to the high-mobility and small bulk band gap, produces a spin Hall conductivity that exceeds other previously mentioned materials by almost two orders of magnitude[74]. Therefore, given both the progress and the current results, summarized in Fig. 6, topological materials possess a significant amount of promise in magnetic device technologies, such as MRAM. In Fig. 6a, we plot both the electrical and spin Hall conductivities for commonly used metals with strong spin–orbit interactions along with TIs. It is clear that the metals are more electrically conductive than the TIs, due to the much larger band gaps observed in TI and the larger density of states in the metals. As the metals featured in Fig. 6a are well known to have strong spin–orbit interactions, it is not surprising that they also have a large spin Hall conductivity. However, in TIs with smaller band gaps, like $Bi_{0.9}Sb_{0.1}$, measurements have shown that not only are TIs capable of producing spin Hall conductivities that are greater than metals by, in some cases, two orders of magnitude but also that TIs produce similar electrical conductivities to metals[74]. We further quantify the significant potential of TIs as SOT materials in Fig. 6b where we plot the experimentally obtained spin Hall angle for the same set of materials in order to demonstrate the spin to charge conversion efficiency of TIs[74]. Once again, TIs have been measured to produce spin responses that far exceed those measured in conventional metals thereby solidifying them as a strong candidate for future MRAM or other magnetic switching device technologies.
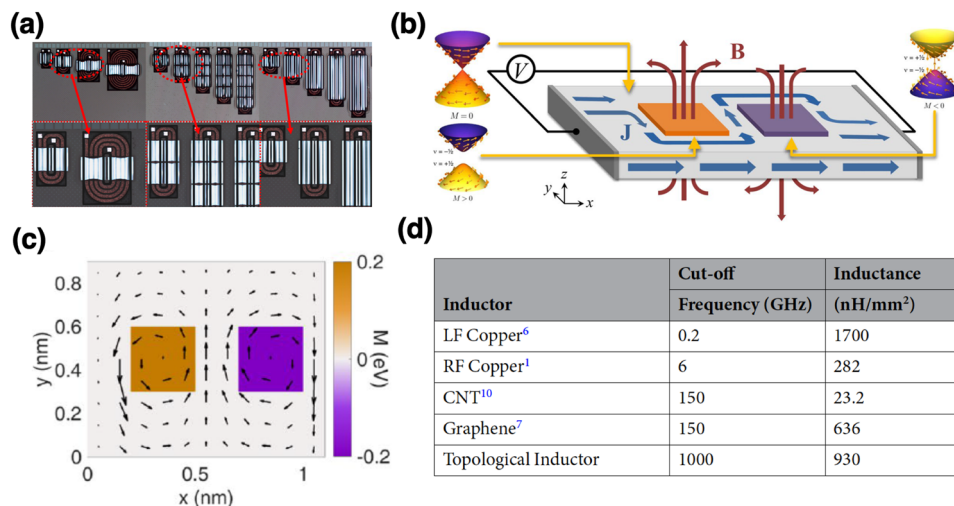
Fig. 7 Topological magneto-electric effect inductors. a Micrographs of $Ni_{45}Fe_{55}$ inductor elements as fabricated by physical vapor deposition. Reprinted from ref. [76], with the permission of AIP Publishing. **b** Theoretical schematic of a novel inductor structure that utilizes antiferromagnetically ordered ferromagnetic islands on the surface to induce magneto-electric responses and transduce energy[75]. **c** The current density on the surface of a topological inductor near the antiferromagnetically ordered islands showing the current forming a vortex[75]. **d** Table comparing various state-of-the-art inductor technologies illustrating the potential of topological materials in passive magnetic electronic devices.[75]. Reprinted by permission from ref. [75], copyright 2017.

Magneto-electric effect-based topological device technologies. A common assumption is that the issues of SWaP may be circumvented by the design of a better transistor. Unfortunately, better transistors would deliver only incremental improvements as these components are already highly optimized in technology. On the other hand, better filters and better passive components could potentially advance the state of the art by orders of magnitude. With this in mind, historically, it has been possible to reduce the size of active CMOS devices to ≈10 nm dimensions, and passive energy-storage devices (inductors and capacitors) have not seen the same reduction in size[1]. Of the passive devices (e.g., resistors, capacitors, and inductors) used in CMOS technologies, the circuit element that consumes the most area on an integrated circuit while simultaneously finding the least success in miniaturization is the inductor. Inductors are fundamental circuit elements that store magnetic field energy when a current is passed through them due to the fact that any changing current creates a change in the magnetic flux that, in turn, induces a voltage across the inductor. Common incarnations of inductors found in current semiconductor implementations utilize small wires fabricated on the surface of semiconductor chips in a spiral pattern using highly conductive metallic wires, most prominently copper wires.

Unfortunately, existing inductors suffer from several significant problems that limit their usage. The first problem is that current inductors have very low inductances (<10 nH), and thus additional magnetic materials must be added to improve the energy storage. However, only select magnetic materials may be used to ensure that the inductors operate within the desired frequency range. In typical ferromagnetic materials, the operating frequency is limited to ≈2 GHz due to the magneto-crystalline anisotropy fields that limit the ability of magnetic domains to follow high-frequency pulses[75]. To date, the most efficient on-chip inductors are fabricated using $Ni_{45}Fe_{55}$ that has both a large magnetic moment and inductive resistivity, but the performance of these on-chip inductors, as shown in Fig. 7a, remains only between 4x and 6x better than the typical inductor with air-core yokes[76]. While other materials with a larger magnetic moment (Fe-N, Co-Ta-Zr, etc.) have been attempted in inductor yokes, the standard deposition techniques have not been amenable to the use of these materials, and little progress has been achieved. In concert, these constraints have made high-quality on-chip inductors difficult to manufacture for inclusion in high-performance nanoscale radio frequency circuits[76]. Furthermore, the prospects of scaling inductors using current materials and designs are complicated by the fact that, as the metal traces that comprise the inductor approach the nanometer scale, their inherent resistance becomes much larger, severely constricting the performance[77] necessitating a search for new solutions supported by different physical principles.

Beyond the spin–momentum locking of the surface states in topological materials, they also possess a unique coupling between their electromagnetic properties, known as the magneto-electric effect, that may be important in the design of future devices in which electricity and magnetism interact with one another, such as inductors. The magneto-electric effect in a topological material is a non-linear current response that arises due to the coupling of both the electric, **E**, *and* magnetic, **B**, fields in a given material. In other words, due to the presence of the strong magneto–electric coupling, when an electric field is applied to a topological material, there is a corresponding magnetic response and vice versa. Recent theoretical efforts have revealed that, by pairing topological materials with ferromagnetic domains[75,78], it is possible to create highly efficient inductive structures capable of satiating the above listed issues with current inductor technology. In such a device, alternating ferromagnetic domains on the surface form a long-range ordered antiferromagnetic pattern on the surface of the 3D TI, Bi_2Se_3[75], to form a new type of inductor structure, as shown schematically in Fig. 7b. The presence of the magnetism breaks the underlying time-reversal symmetry such that a dynamic magneto–electric effect is generated in which the magnitude of the coupling between the electric and magnetic fields is spatially varying[79]. When an alternating current (ac) current is applied to the topological inductor, the electric field generates a surface current that is bent around the magnetic domains by the magnetic field generated by the TI. In Fig. 7c, we see the result demonstrating that the bend of the current from the ac current forms a circulating pattern around the magnetic domains thereby transducing energy from the applied electric field into the magnetic field generated by the

circulating current as calculated using a unique computational technique that combines the consistent solution of quantum mechanical Green's functions and electrodynamic equations[80]. In order to demonstrate the potential that the magneto-electric effect may have in passive magnetic electronics, we benchmark the performance, albeit theoretical, of the topological inductor against other emergent technologies and current copper inductors. In Fig. 7d, we plot two important metrics for inductors, cutoff frequency (frequency at which the inductor ceases operation) and the inductance density. From the table, it is clear that copper at low frequency, below 1 GHz, performs best though scaling problems presented in "Topological electronic devices" may determine how much scaling these may undergo. At higher frequencies, the skin effect in copper and ferromagnetic permeability resonance degradation cause significant decreases in both the cutoff frequency and the inductance density[81]. Alternatives to copper are offered by carbon-based solutions in the form of nanotubes[82] and graphene[83]. Clearly, the cutoff frequency improves dramatically; however, both of these carbon designs suffer from an anomalous skin effect, or an analog of the skin effect in materials with higher mean-free paths, that serves to limit their ultimate applicability at frequencies >150 GHz. In this sense, the topological inductor shows significant promise as an inductor with a cutoff frequency and inductance density that exceeds the other proposed technologies. By extension, the example of the topological inductor illustrates the potential of TI in the area of passive magnetic device technology via the exploitation of the magneto-electric effect.

Summary and outlook

In this review, we have attempted to survey the vast and continuously expanding landscape of topological materials within the context of new device technologies utilizing properties of "well-known" TIs. The guiding principle behind this review has been to illustrate how the unique physical principles that arise due to the presence of topology may play a significant, if not, defining role in the development of new electronic, magnetic, or magnetoelectric information device processing technologies. To this end, we have only focused on the aforementioned materials of Bi_2Se_3 and Bi_2Te_3. These materials are singularly the focus due to the fact that the existing condensed matter and materials studies have elucidated many of the most salient properties of these materials both that stem from the topological and non-topological effects. Accordingly, these materials have had sufficient time to mature to the point where they may now be routinely produced at a high-quality level that is sufficient for wider distribution as, from the condensed matter perspective, many of the most impactful measurements have been made. In the sense that these topological materials are well explored and mature, it is our estimation that they possess sufficiently interesting physical properties that they may have an impact on future information processing device technologies and that it is necessary for the device engineers to perform their exploration of these materials.

We have shown that desirable properties of TIs have improved greatly as a function of year, yet, their electronic device performance still lags behind current implementations of CMOS technology. Given the costs that are associated with a change in base material from silicon or closely related compounds, it is difficult to see TIs playing a role in CMOS-type architectures as the improvements possible in SWaP do not justify such a change. On the other hand, we have shown that TIs are a particularly attractive candidate for magnetic device technologies that may far outperform other competing technologies given both the rate of improvement in materials and performance metrics. To this end,

the exploration and optimization of the magnetoelectric response in TRI topological materials represents a clear and present research opportunity with great potential for use in new magnetic device technologies. In conjunction with any of these topological phenomena, and the primary motivation for the construction of this review, is that engineering analysis of device structures and geometries must be undertaken. Measurements typically undertaken in many of the engineering buildings must be applied to understand the device limits and issues surrounding topological devices. Engineering issues such as contact materials, frequency responses, device parasitics, and device processing must be understood before a final verdict of ultimate viability is rendered on topological materials for future device concepts. As "well-known" topological materials depart the realm of condensed matter for engineering, there will undoubtedly be new advances and breakthroughs certain to keep these interesting materials at the forefront of research for many years to come.

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Acknowledgements

Competing interests

The author declares no competing interests.

Additional information

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