nature reviews electrical engineering

https://doi.org/10.1038/s44287-024-00038-5

Review article

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3D integration of 2D electronics

Darsith Jayachandran[1,5] ✉, Najam U Sakib[1] & Saptarshi Das[1,2,3,4] ✉

Abstract

The adoption of three-dimensional (3D) integration has revolutionized NAND flash memory technology, and a similar transformative potential exists for logic circuits, by stacking transistors into the third dimension. This pivotal shift towards 3D integration of logic arrives on the heels of substantial improvements in silicon device structures and their subsequent scaling in size and performance. Yet, advanced scaling requires ultrathin semiconducting channels, which are difficult to achieve using silicon. In this context, field-effect transistors based on two-dimensional (2D) semiconductors have drawn notable attention owing to their atomically thin nature and impressive performance milestones. In addition, 2D materials offer a broader spectrum of functionalities — such as optical, chemical and biological sensing — that extends their utility beyond simple 'more Moore' dimensional scaling and enables the development of 'more than Moore' technologies. Thus, 3D integration of 2D electronics could bring us unanticipated discoveries, leading to sustainable and energy-efficient computing systems. In this Review, we explore the progress, challenges and future opportunities for 3D integration of 2D electronics.

Sections

[1]Department of Engineering Science and Mechanics, The Pennsylvania State University, University Park, PA, USA. [2]Department of Electrical Engineering, The Pennsylvania State University, University Park, PA, USA. [3]Department of Materials Science and Engineering, The Pennsylvania State University, University Park, PA, USA. [4]Materials Research Institute, The Pennsylvania State University, University Park, PA, USA. [5]Present address: IBM Research, Albany, NY, USA. ✉e-mail: darsith.jayachandran@ibm.com; sud70@psu.edu

Key points

- 2D electronics must overcome several challenges before they can be adopted in commercial semiconductor chips. Some of the major challenges are discussed in the section 'Towards very-large-scale integration of 2D electronics'.
- Research efforts in 2D material synthesis and device integration strategies must happen synergistically, with the goal of 3D integration, because silicon technology is already mature, with the most advanced nodes reaching the limits of planar integration in gate-all-around field-effect transistors.
- 3D integration with 2D electronics not only demands the maturity of 2D electronics in the planar dimension but also poses new difficulties in the vertical direction. These difficulties must be thoroughly understood and addressed before 2D materials can be introduced into commercial electronics.
- 2D materials have the potential to enable multifunctional chips by combining logic with memory and sensing in a 3D-integrated chip. Multifunctional chips containing 2D electronics should be developed with the goal of manufacturing task-specific semiconductor chips and thereby addressing various integration challenges.

Introduction

The unification of metal–oxide–semiconductor field-effect transistors (MOSFETs) with the concept of universal Turing machines in modern computer science marked a substantial milestone in the advance of digital electronics and technology. The desire to minimize the size and power requirements of computers demanded faster and more compact electronic circuits[1]. Moreover, Gordon Moore's prediction that the number of transistors on a chip would double approximately every two years spurred semiconductor industries to compete in a race to adhere to this trend, known as Moore's law[2]. This marked the beginning of an era dedicated to achieving maximal scaling in size and power efficiency of semiconductor chips, with the number of transistors per chip escalating from a few thousand to billions in less than five decades[3]. At present, scaling in semiconductor technology encompasses two primary aspects: (1) scaling based on system-level integration to augment the transistor count per chip and to incorporate additional functionalities into a system-on-a-chip and (2) scaling focused on the individual dimensions, structure and density of transistors[4].

To facilitate scaling based on system-level integration, several semiconductor industries have developed various 3D integrated circuit (IC) packaging techniques[5] and integration solutions[6], such as Intel's Foveros technology[7] and TSMC's 3DFabric, which utilize system-on-integrated-chips technology[8]. This arena of scaling thrives on innovations in technologies like wire bonding, through-silicon vias, through-glass vias, face-to-face chip stacking, flip-chip and the ThruChip interface[9]. These technologies enable increased interconnect bandwidth, enhanced performance, power and area, and potentially reduced costs, especially when stacking chiplets[10]. Conversely, the International Roadmap for Devices and Systems predicts that future process nodes will require highly parallel 3D architectures, achievable only through the sequential stacking of individual devices on top of one another[11]. Note that the term 'node' is not used to refer to the smallest features that can be reliably manufactured, as was in the case of planar transistors, but to denote a new generation of process technology and devices that offer better performance and efficiency than their predecessors. This technique, known as monolithic 3D integration, involves the fabrication of thinner functional tiers separated by interlayer dielectrics and interconnected via monolithic inter-tier vias[12]. Several predictions and analyses already highlight the opportunities and advantages of monolithic 3D integration, including increased interconnect density, reduced electrical parasitic capacitance, enhanced energy efficiency and better performance[13–16]. The future technologies will integrate novel 3D IC packaging and integration solutions with monolithically 3D-integrated individual chips.

It is interesting to note that, despite its conception in the 1980s[17–19], initial research on 3D integration was not actively pursued. This lack of interest was due to the then-prevalent trend of downsizing individual silicon-based transistor dimensions — a process made feasible through advances in materials science, electronics and nanofabrication. Consequently, transistor device dimensions shrank dramatically, transitioning from the micrometre regime to the realm of tens of nanometres. This period marked the introduction of high-κ dielectrics and strained silicon technology, as well as a shift from the classical planar field-effect transistor (FET) structure to newly emerging architectures. These include non-planar fin-shaped FETs (finFETs), gate-all-around (GAA) FETs (also known as nanosheet FETs, ribbon FETs, and multi-bridge channel FETs), and the potentially forthcoming forksheet FETs and complementary-FETs[20–22]. This evolution, which began in 1959, is depicted in Fig. 1a. However, it is challenging to scale transistors down further by reducing the thicknesses of semiconductor channels to less than 3 nm, because of inherent issues in silicon and other bulk semiconductors, such as increased charge carrier scattering at the semiconductor–insulator interface and subsequent mobility degradation[23,24]. Along these lines, among other contenders such as carbon nanotubes and nanowires, ultrathin 2D semiconductors emerge as promising materials to facilitate the continued miniaturization of transistor dimensions[25].

From a materials perspective, 2D semiconductors, particularly transition-metal dichalcogenides (TMDs), have drawn tremendous attention in the past decade with demonstrations of high-quality wafer-scale synthesis, high-performance FETs, in-sensor and in-memory computing, optical, biological and chemical sensors, scaled FETs, and so on[26–28]. The progression in the development of growth technologies[29–34] for 2D TMDs and the performance of their electronic devices[35–43] is illustrated in Fig. 1b. Apart from that, 2D materials also have applications in twistronics, spintronics, straintronics, valleytronics and flexible electronics[44–48]. Hence, as shown in Fig. 2, 3D integration with 2D electronics not only presents alternative pathways for scaling individual devices in line with the 'more Moore' approach (continued scaling in accordance with Moore's law) but also provides diverse functionalities that can be leveraged to co-design and incorporate non-computational devices within the same platform, facilitating the realization of 'more than Moore' technologies[49]. In addition, theoretical studies have predicted that incorporating 2D electronics into monolithically integrated 3D chips can increase the integration density[50].

Here, we review the progress towards 3D integration of 2D electronics and its prospects and challenges. The review begins with a section on progress and challenges towards very-large-scale integration (VLSI) of 2D electronics followed by a summary of various 3D IC demonstrations that use 2D materials. Finally, we conclude this Review with a section on comprehensive device design considerations and the associated challenges.

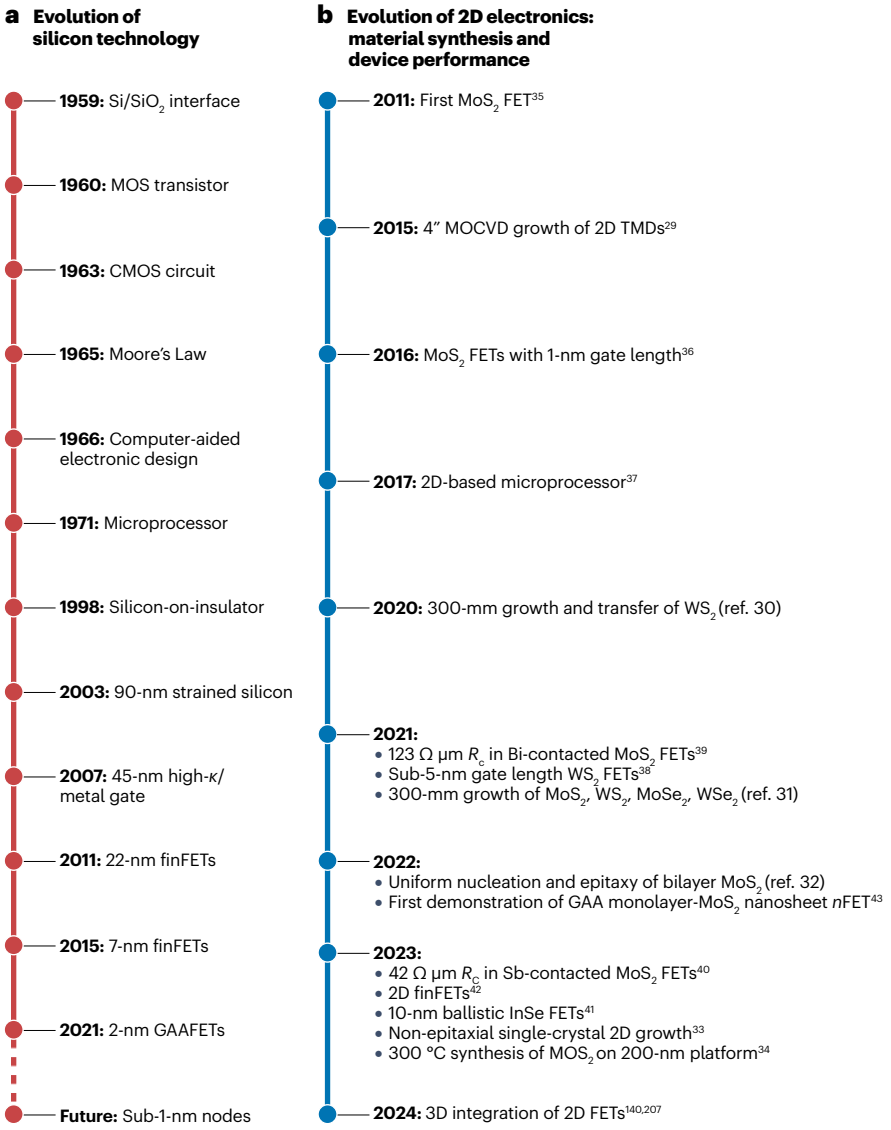

Fig. 1 | Evolution of silicon technology and 2D electronics. a, Evolution of silicon-based transistor technology highlighting key milestones achieved since 1959. **b**, Evolution of 2D electronics: material synthesis and device performance. Although the first 2D material — graphene — was discovered in 2004, it was not until 2011 that the first transistor based on a 2D semiconductor was demonstrated. Since then, the performance of 2D-based field-effect transistors (FETs) has substantially improved, surpassing existing silicon technology in some instances. MOS, metal–oxide–semiconductor; CMOS, complementary metal–oxide–semiconductor; MoS_2, molybdenum disulphide; $MoSe_2$, molybdenum diselenide; MOCVD, metal–organic chemical vapour deposition; WS_2, tungsten disulphide; R_C, contact resistance; κ, the dielectric constant; TMD, transition-metal dichalcogenides. Data are taken from refs. 29–43,140,207.

Towards very-large-scale integration of 2D electronics

Here, we succinctly highlight the advances in various facets of 2D electronics, while simultaneously addressing the immediate challenges that need to be met. Overcoming these obstacles is imperative for the eventual realization of industrial-scale production of 2D-based 3D ICs.

Material synthesis

Growth techniques for 2D materials have evolved considerably from mechanical exfoliation since the discovery of graphene. Initially, wafer-scale synthesis efforts included the chemical vapour deposition (CVD) of MoS_2 on SiO_2 substrates, achieving millimetre-scale coverage[51,52]. By 2015, MoS_2 and WS_2 synthesis expanded to 4-inch SiO_2/Si wafers using metal–organic chemical vapour deposition (MOCVD). Simultaneously, the synthesis of MoS_2 on other substrates, such as Al_2O_3, HfO_2 and SiN, was also reported[29]. In 2017, IMEC used atomic layer deposition (ALD) or plasma-enhanced CVD to fabricate back-end-of-line (BEOL) compatible WS_2 transistors on 300-mm SiO_2/Si wafers[53]. In 2018, ~6-inch batch production of MoS_2 on soda-lime glass via a face-to-face metal-precursor feeding route in a CVD process was demonstrated[54]. In 2021, Intel identified CVD growth from pre-patterned seeds, and MOCVD as leading techniques for synthesizing MoS_2, WSe_2, $MoSe_2$, and WS_2 on 300-mm SiO_2/Si wafers, which provides both transfer and direct deposition options[31]. Concurrently, epitaxial growth of 2D TMDs on sapphire substrates (via CVD or MOCVD) made strides owing to the high quality and uniformity of the synthesized 2D crystals[55,56]. In addition, step engineering of growth substrates and adjustable growth conditions could control the nucleation and growth direction, making it possible to obtain wafer-scale uniform single-crystal films of MoS_2 (refs. 57,58), WS_2 (ref. 59) and WSe_2 (ref. 60). Changing growth conditions can alter the nucleation of 2D materials on step edges, so that it transitions from occurring predominantly at the top edge to the bottom edge of the step, thus shifting the preferred domain orientation. A recent advance has been made in the uniform nucleation and epitaxial growth of bilayer

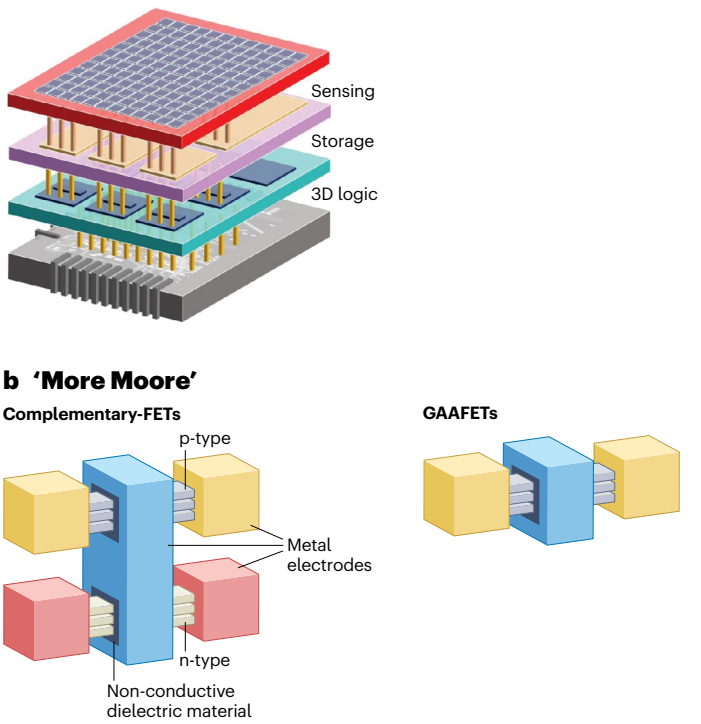

Fig. 2 | 3D Integration of 2D electronics. a, Schematic of 3D integration of 2D electronics: additional functionalities such as sensing and storage with logic can be enabled in a 3D integrated chip based on 2D materials. **b**, 'More Moore'. 2D field-effect transistors (FETs) can provide scaling benefits when introduced in gate-all-around FETs (GAAFETs) (right) and stacked FETs (also known as complementary-FETs) (left). **c**, 'More than Moore'. 2D FETs can also facilitate the integration of non-computational devices within 3D architectures for applications in chemical/bio sensing, optoelectronics and memory. Part **a** reproduced from ref. 207, Springer Nature Limited.

MoS_2, achieving ON-state FET performance that aligns with the International Roadmap for Devices and Systems 2028 objectives[32]. In 2023, non-epitaxial single crystal 2D growth by geometric confinement was demonstrated[33]. Direct growth of MoS_2 on 200-mm silicon complementary metal–oxide–semiconductor (CMOS) circuits at 300 °C (ref. 34), and on flexible substrates such as polymers and ultrathin glasses at 150 °C (ref. 61), aligns well with 3D integration needs because of their low thermal budgets. However, achieving epitaxial quality across all 3D stack tiers is essential for industrialization. Sequential monolithic 3D integration based on the transfer of 2D materials from growth substrates to target chips or wafers could be another option. We note that the underlying substrate properties will be different for the fabrication of the second tier of devices in comparison to the first tier because the fabrication steps and conditions will have to be adjusted in order not to cause any damage to the already fabricated tier-one devices. (Here, the word tier is used to refer to different levels of device). In contrast, the general high temperature and substrate requirements for epitaxial synthesis makes the transfer process promising for 3D stacking. Regardless, controlling film thickness and uniformity, and minimizing defects and contamination during synthesis or transfer, are vital for optimizing the yield and variability of 2D FETs. Furthermore, surface treatments of the 2D channels[31,62] during tier-two fabrication might affect bottom-tier device performance, thus necessitating comprehensive studies on both the 2D-material–contact interfaces and the interlayer-dielectric–2D-material–gate-dielectric interfaces (depending on the device architecture; 2D material will not have an interface with the interlayer dielectric in a gate-all-around architecture, but can form an interface in the case of planar devices) of tier-one devices before and after fabrication of tier-two devices. Although both direct deposition and transfer approaches show potential, the ideal technique for 3D integration of 2D FETs remains to be determined.

Transfer process in 2D electronics

Following epitaxial growth, 2D materials can be transferred from high-temperature growth substrates to desired target substrates (with pre-fabricated back-gate dielectric stack or substrates for top-gate processing) using (1) polymer-assisted wet transfer methods, (2) polymer-free transfer methods or (3) deterministic dry transfer methods[63]. We note that the use of polymers and associated cleaning steps often induces undesirable defects in the 2D films. From an industrial perspective, the ideal technique must enable high-throughput wafer-scale 2D transfers with high yield and clean interfaces. Some of the earlier notable attempts involved transfer of 5-cm-diameter 2D-material wafers[64,65]. Water-based etching-free 6-inch MoS_2 transfer using a ethylene vinyl acetate/polyethylene terephthalate stack was demonstrated in 2018 (ref. 54). Similarly, IMEC has demonstrated 300-mm transfer of WS_2 using temporary wafer-to-wafer bonding and a laser debonding technique[38,66]. In 2022, TSMC utilized evaporated Bi as a gentle adhesive layer to perform 2-inch WS_2 dry transfer[67]. There also exist Au-assisted 2D transfer processes, as shown previously[57,68]. Recently, IMEC developed the collective die-to-wafer (CoD2W) technique and demonstrated a two-step residue-free transfer of both MoS_2 (epitaxial growth on 2-inch sapphire using water intercalation) and WS_2 (grown on SiO_2 with completely dry debonding) to 300-mm target wafers using adhesive-coated glass carriers[69]. From an automation perspective, a notable demonstration involved 100 µm × 100 µm 2D transfer with high speed and precise angle control using a robotic assembly[70]. In addition, 2D FETs suffer from the phenomenon of Fermi-level pinning[71],

which causes the Schottky barrier height at the metal–semiconductor junction to be independent of the metal work function, leading to less control when engineering the contact resistance. Some studies suggest that Fermi-level pinning can be somewhat alleviated by minimizing the defects in the 2D channel during contact deposition[72–74]. As a result, the technique of transferring pre-assembled arrays of metal contacts onto the 2D semiconductor is becoming a promising alternative for contact engineering[74–78]. Similarly, there have been various demonstrations of dielectric transfer[79–81]. These demonstrations, including those from industry, point towards the potential of the transfer process as a scalable integration step in 2D electronics.

To effectively execute a transfer strategy for 2D electronics, several crucial metrics must be considered. These include the ability to transfer large-area films at the wafer level while ensuring the structural integrity of the transferred films. Achieving scalability and automation is imperative for industry acceptance. Additionally, the interface of the transferred 2D material and the target substrate should not contain defects or contaminants. Uniformity and reproducibility across the entire wafer, minimizing device-to-device variation, are critical for reliable outcomes. But we note that, even though transfer techniques show promise, an ideal scenario would involve high-quality growth of 2D materials at BEOL-compatible temperatures.

Threshold voltage engineering

Managing the threshold voltage (V_{TH}) of a FET allows control over its ON-state. This critical parameter depends on factors such as the gate dielectric, the work function of the gate metal, and the unintentional or intrinsic doping within the 2D material. In the realm of digital circuits designed for low power consumption, minimizing the V_{TH} is paramount. With increasing chip density, there has been a corresponding rise in power consumption, resulting in undesirable levels of heat generation. In this context, maintaining a low operating voltage is crucial, which requires precise control over V_{TH} for both *n*-type and *p*-type FETs. Furthermore, CMOS circuits demonstrate optimal performance only when the V_{TH} for both *n*-type and *p*-type FETs are carefully calibrated. Suboptimal V_{TH} values can substantially affect signal propagation within CMOS circuits. Overall, V_{TH} engineering is vital to meet the specific requirements of various electronic applications. In Si-based CMOS technology, doping in the semiconductor channel and altering the work function of the gate electrode material are used for finely tuning V_{TH}. However, comparable progress in V_{TH} engineering of 2D electronics is still limited. Techniques such as substitutional doping and surface charge-transfer doping (SCTD) can be used to control the V_{TH} of a 2D FET. Substitutional doping involves the substitution of cationic and anionic elements with foreign atoms that have similar radii[82]. For *p*-type doping, cationic elements like niobium (Nb), tantalum (Ta) and vanadium (V) can be used, while rhenium (Re), hafnium (Hf), and zirconium (Zr) are utilized for *n*-type doping[83–87]. Despite demonstrations of devices utilizing doped TMDs[88–91], achieving a uniform impurity density and precise control at large scale, while using methods compatible with state-of-the-art Si CMOS process lines, still presents a substantial challenge. The V_{TH} in *p*-type WSe_2 FETs can be modulated by adjusting the percentage of V atom doping[85]. This modulation was achieved by precisely controlling the partial pressure of precursors during MOCVD growth. Another challenge with substitutional doping of 2D materials arises from the fact that the ionization energy of dopants is substantially higher (by an order of magnitude) than their ionization energies in bulk semiconductors. This discrepancy is attributed to the quantum confinement effects observed in 2D materials. Consequently, dopant concentrations exceeding one atomic per cent, which far surpass the levels used in traditional doping, are necessary to alter the transport properties of 2D TMDs. Such high doping concentrations can degrade the field-effect mobility of the devices owing to an increase in scattering centres. The exact doping concentration required for mobility degradation cannot be stated because it is influenced by various factors, such as the nature of the dopant atom (atomic mass) and the characteristics of the 2D film[92]. Limited research has been conducted into the impact of doping concentration on mobility degradation, making it a prospective area for future investigation. This issue could be mitigated if the dopant were to create shallower donor levels, allowing for easier carrier activation. In this regard, Re is a transition metal known to form shallow donor levels with MoS_2 (refs. 93,94). MoS_2 monolayers can be *n*-doped by substituting Mo with Re atoms, achieving controllable concentrations down to 500 parts per million using MOCVD[87]. Their findings demonstrated that an increase in Re concentration led to a reduction in the number of sulfur (S) vacancies, resulting in a shift in V_{TH} and subsequently enhanced device performance. The higher free energy of formation of S vacancies as a result of Re doping has been claimed to be the reason for fewer S vacancies. This substitutional approach can also be extended to anionic replacement[95–97].

Another doping approach for modulating V_{TH} of devices is SCTD. For the effective implementation of the SCTD approach, it is essential to meticulously design the gate stack. This design should ensure three key aspects: (1) the equivalent oxide thickness (EOT) must remain unaffected, (2) the gate control should be maintained, and (3) the channel material must not suffer any damage. In SCTD, dopant atoms are attached to the 2D material through either a chemical bond or a physical interaction, resulting in a charge-transfer process. The direction of charge transfer is determined by the Fermi-level difference between the dopant and the host materials, dictating whether the adsorbed dopant functions as an acceptor or a donor. Unlike substitutional doping, SCTD does not introduce any lattice disorders, because dopants are positioned outside the electrical carrier pathways. As a result, SCTD in general enables the retention of higher electrical mobility in the 2D materials. SCTD has been successfully demonstrated in various TMDs, allowing for both *n*- and *p*-type doping with different degrees of effectiveness[98,99].

Additionally, ozone or oxygen plasma treatment can be applied to transform the top layer of TMDs into their corresponding sub-stoichiometric oxides, resulting in substantial *p*-type doping in the layers below[100]. The previous study shows that converting atomically thin WSe_2 to WO_x led to strong hole-doping owing to electron transfer from the underlying WSe_2 to the surface WO_x (ref. 101). Doping can also be induced by depositing a sub-stoichiometric insulator on top of the 2D material. This doping can occur through two processes. The first involves the transfer of charge due to trap states at the semiconductor/oxide interface or in the oxide near the interface (such as border traps). The second process involves doping the 2D material via the transfer of electrons or holes from states that do not overlap with the energy gap of the 2D semiconductor. The challenge lies in achieving doping through this latter process, given that it does not degrade the subthreshold slope and mobility of the device. It has been demonstrated that an improvement in the device performance can be achieved, along with a large V_{TH} shift of around 20 V, by depositing aluminium oxide[102]. Other oxides, like amorphous titanium suboxide[103], molybdenum trioxide[100,101,104] and silicon nitride[105] have also exhibited similar behaviour. These avenues hold promise for addressing the V_{TH} engineering challenges in both *n*- and *p*-type 2D FETs, a crucial

step towards realizing 2D CMOS circuits. Studies have also explored tuning the threshold voltage by incorporating an interfacial layer in the gate dielectric, with a predominant focus on silicon. As a result, a shift in flat band voltage can be obtained by introducing titanium (Ti) and Hf in a metal/high-κ gate stack[106]. Even though there is a scarcity of research on 2D materials concerning the dipoles originating from the gate dielectric, research into dipoles induced by organic polymers, capable of altering the threshold voltage in 2D materials, has been conducted[92,107,108]. In another study, gadolinium aluminate was used in the dielectric stack to gain control over the threshold voltage[109].

In addition to all this, it is also important to note that device-to-device variation can stem from defects in the as-grown 2D material or at the interface between the 2D material and the dielectric. Acceptable device-to-device variability is thus a crucial milestone for 2D electronics which is yet to be achieved[110]. Thus, threshold voltage engineering techniques must be developed hand-in-hand with interface engineering and a focus towards reducing device-to-device variation on the large scale.

Yield, variability and dielectric integration

In addition to V_{TH} engineering, achieving high device yield and minimizing device-to-device variability are other crucial prerequisites when designing and demonstrating large-scale CMOS circuits. While device yield affects the effective design of integrated circuits, such as the footprint, uniformity in device performance is essential for the proper operation of CMOS circuits (achieving correct voltage levels).

Transferring synthesized 2D materials poses challenges owing to their atomically thin and exceedingly delicate structure. Moreover, the capillary forces that arise when the film is removed from the solution bath can cause the material to wrinkle, fold and crack. Conversely, direct growth of 2D materials on substrates suitable for commercial applications is often constrained by the requirement for high growth temperatures, the use of chemically reactive precursors and the need for epitaxial alignment. Such elevated growth temperatures can cause the deterioration of the underlying substrate, thereby adversely affecting device performance and reliability[111–113].

To improve the yield and reliability of 2D FETs, in addition to fine-tuning or eliminating the transfer process, there is a need for comprehensive optimization in both the growth of 2D materials and process integration. The growth of 2D materials must be a very precise and controlled process in order to control the quantity of vacancies and defects, with the ultimate goal of ensuring that the as-grown material exhibits minimal vacancies and defects. A uniform crystalline film is also essential to achieve good yield and better reliability. The number and distribution of grain boundaries can play a part in determining both the performance and uniformity of devices. Devices that are smaller than the average grain size tend to be less affected by these boundaries, whereas larger devices are more susceptible to their influence. In particular, a device located directly on a grain boundary can experience pronounced effects. The variability in device characteristics, especially when comparing devices with different numbers of grain boundaries, is an important consideration. However, this variability can be mitigated by increasing the grain size and improving the growth process, thereby making the material more uniform. While addressing the challenges posed by grain boundaries is an ongoing area of research, it is worth noting that they might not necessarily be a limiting factor in device variation. This is especially true given the sizes of domain typically achieved in current 2D-material growth techniques. Additionally, on a circuit level, the tolerance for device-level variability tends to be higher. Circuits can often accommodate a certain degree of variation in individual components without notable loss of overall functionality. This inherent resilience could mean that grain boundaries, although a critical factor in device variation, might not be a critical obstacle. Therefore, although grain boundaries can contribute to device variability, their eefect might be less critical at the circuit level. Continued research and development in material growth and processing techniques will further clarify their role and potential ways to mitigate their effects on device performance. Therefore, grain boundaries are a crucial factor to consider, but they do not inherently preclude the effective use of 2D materials in scaled devices.

Additionally, mitigating device variability involves fine-tuning contact formation, optimizing the integration of gate dielectrics and incorporating effective post-fabrication device treatments or annealing steps. In this context, it is worth noting a study[110] in which the effect of imperfections of individual FETs on 2D-based electronic circuits was thoroughly examined. The authors emphasize the importance of electrically active traps that can arise from defects at various points in the FET structure, such as the channel, the dielectric and the interface between the channel and the dielectric. These traps can introduce variability in V_{TH} of individual devices, underscoring the need for meticulous optimization. Thus, the advances towards the development of high-density 3D CMOS circuits built upon 2D FETs must also prioritize enhancing yield through the optimization of synthesis, transfer and fabrication processes. Equally crucial is the selection of a compatible 2D-material–dielectric combination that minimizes device-to-device variability. Even though device variability was not studied, there has recently been some work on incorporating crystalline dielectrics such as CaF_2 (ref. 114) and $SrTiO_3$ (ref. 79) with low EOT in 2D electronics.

In addition, the integration of ultrathin high-κ dielectrics with 2D materials is a crucial component, particularly in GAA device architectures. To achieve successful integration of scaled dielectrics, two critical factors are essential: low leakage currents (less than 10^{-2} A cm^{-2}) and high dielectric strength (greater than 10 MV cm^{-1})[115,116]. The attainment of these characteristics is closely tied to having a high dielectric constant and a large bandgap. Noteworthy materials that meet these specifications include HfO_2, with a dielectric constant of approximately 23, and CaF_2, with a bandgap of around 12 eV. It is important to highlight that within this context, the physical thickness of the dielectric layer is not as vital as the EOT. The primary objective is to minimize the EOT to less than 1 nm. Substantial strides have been made towards this objective, such as the achievement of reducing HfO_2 thickness to attain an EOT of less than 1 nm, alongside an impressive ON-state current (I_{ON}) performance of approximately 420 μA μm^{-1} in a dual-gated MoS_2 MOSFET configuration. This approach incorporated an interfacial layer of gadolinium aluminate within the dielectric stack, thereby enabling effective V_{TH} control and enhancing carrier transport properties[109]. Additionally, the capability to achieve an EOT of 1 nm for graphene, MoS_2, and WSe_2 devices has been demonstrated, attributed to the use of an ultrathin (~0.3 nm) layer of perylene-tetracarboxylic dianhydride (PTCDA) molecular crystals as a seeding layer. CaF_2 insulators could also enable scaling down to less than 1 nm EOT (with a physical thickness of 2 nm), thereby achieving not only low leakage currents but also competitive device performance, including a subthreshold swing down to 90 mV dec^{-1} (ref. 117). These advances underscore the importance of novel approaches in the pursuit of scaled dielectrics with enhanced electrical properties. Apart from that, GAA deposition techniques for 2D materials have been demonstrated, but further exploration into integration challenges such as the damage to the 2D

channels during gate-stack or contact formation is necessary[118]. GAA single-layer MoS_2 devices, for instance, have shown an I_{ON} of 410 μA μm^{-1} and a subthreshold swing of 220 mV dec^{-1}, indicating the viability of GAA architectures for 2D materials[43]. However, the variety of dielectric stacks and gate metals used in various studies makes direct comparison of the findings challenging. Therefore, a new parameter, the projected threshold voltage variation ($S\sigma V_{TH}$), has been introduced to facilitate comparisons across various studies on 2D materials and with the silicon industry[119]. As a result, a relatively low $S\sigma V_{TH}$ value of 33 mV was obtained, compared with those of state-of-the-art ultra-thin-body silicon-on-insulator and silicon finFETs, which were 13 and 20 mV, respectively[120,121]. Addressing the concerns discussed in this section is pivotal for further improvements in reducing threshold voltage variation.

Device performance

Despite various advances, the performance of 2D FETs is still hindered by contact limitations. The primary issue revolves around achieving contacts that demonstrate ohmic behaviour. In contrast to silicon-based devices, where low-resistance ohmic contacts are obtained through precise doping via ion implantation of the underlying silicon beneath the metal, replicating such results in 2D materials is hindered by their atomically thin nature. Additionally, the process of engineering contacts for 2D materials is further complicated by phenomena such as Fermi level pinning[71]. Ongoing research in the field of 2D materials has recently led to breakthroughs demonstrating ultralow contact resistance in these materials, surpassing the capabilities of traditional silicon-based CMOS technologies and meeting the targets set for 2028 by the International Roadmap for Devices and Systems. A notable achievement includes the realization of ultralow contact resistance of 123 Ω μm using bismuth (Bi) contacts[39]. However, it is not practical to use Bi owing to its low melting point (below 300 °C), prompting a shift towards antimony (Sb) as a more viable contact metal for MoS_2 thanks to its higher melting point (above 600 °C). This switch has enabled the demonstration of ultralow contact resistance of 42 Ω μm (ref. 40) and reported currents exceeding 1 mA μm^{-1}. Further progress has been seen in achieving the on-state current (I_{ON}) of 1.27 mA μm^{-1} (at a drain-to-source voltage of 2.5 V) in short-channel (50 nm) FETs based on bilayer MoS_2.

In another report, the FETs made from mechanically exfoliated InSe flakes showed ballistic transport achieved by using a phase-transition method induced by yttrium doping[122]. The channel length could be scaled down to 10 nm while attaining a contact resistance as low as 62 Ω μm. Although these results hold promise, further exploration is required for reproducibly achieving such high performance on a larger scale. Furthermore, the successful integration of large-scale 2D CMOS requires comparable performance from both *n*-FETs and *p*-FETs. While substantial progress has been made in achieving high ON currents for *n*-type 2D FETs, replicating these successes for *p*-type counterparts has presented remarkable challenges as given below.

p-type 2D FETs

Two major obstacles towards *p*-type 2D FETs include Fermi-level pinning and substrate-induced electron doping by charge transfer[123]. The Fermi-level pinning is generally believed to be caused by (1) defects in the metal–semiconductor interface (which could be intrinsic defects in the 2D semiconductor, defects generated with the deposition process, adsorbates or other contaminants), (2) strain at the metal–semiconductor interface causing bandgap changes, or (3) reduction of the metal work function due to the formation of interface dipoles caused by the electron density redistribution at the metal–semiconductor junction. In addition to Fermi-level pinning, substrate induced charge transfer electron doping of 2D semiconductors is also observed, which can be caused by impurities or atomic vacancies in the dielectrics[123]. In most cases, the above-mentioned effects are unfavourable for achieving hole transport and thus, 'purely' *p*-type 2D FETs (without any *n*-branch). However, some recently published research aimed to achieve *p*-type 2D FETs with either substitutional doping (mentioned in the section 'Threshold voltage engineering') or contact engineering strategies. In terms of contact engineering, transferring high-work-function metals in van der Waals metal–semiconductor junctions has helped to achieve better hole transport[74,76,78]. Inserting a buffer material such as In or Se between the semiconductor and contact metal was also used to achieve clean and less-damaged contacts[73,124]. Another route, distinct from the above-mentioned techniques, is the treatment of WSe_2 after growth to achieve hole transport. For example, oxygen plasma treatment on transferred WSe_2 flakes[125], immersion of WSe_2 in an aqueous solution of 4-nitrobenzenediazonium tetrafluoroborate (4-NBD)[126] and exposing WSe_2 devices to nitric oxide gas flow[62], have all helped to achieve *p*-type 2D FETs. In another distinct approach, VSe_2 was grown on WSe_2, followed by the formation of cracks to achieve small channel *p*-type FETs with atomically clean interfaces[127]. Recently, another demonstration involved *p*-type electrical contacts for 2D TMDs such as (exfoliated) WSe_2 fabricated with industry-compatible electron-beam evaporation of high-work-function metals such as Pd and Pt[72]. Though promising, more such efforts are required in order to improve *p*-FETs and reach the performance levels of 2D *n*-FETs. Only then, can we achieve 2D CMOS, which can evolve to VLSI of 3D CMOS with 2D electronics.

The above discussion has provided insights into advances in 2D semiconductor research, encompassing contributions from both academic and corporate research environments. Leading semiconductor giants such as Intel and TSMC have notably incorporated 2D materials into their roadmaps. Corporate research initiatives in the field of 2D semiconductors are outlined in Box 1, offering an overview of some of their key findings and accomplishments to date (including some reports that have been discussed above). Recently, Intel also published an article on their perspective on 2D transistors including discussions on challenges and strategies associated with deposition of 2D materials, formation of stacked 2D nanoribbon channels, doping, gate-dielectric/contact formation and contact resistance[118].

Researchers in the 2D electronics field must establish realistic objectives. For silicon-based technologies, these targets are typically provided by the International Roadmap for Devices and Systems. In the realm of 2D electronics, a comprehensive set of targets has been identified, outlining intermediate, critical and long-term goals for 2D transistors. These targets are crucial for the transition from laboratory to real-world applications[128]. Specifically, the critical targets for high-performance I_{ON}, low-performance I_{ON}, mobility (μ), external resistance and subthreshold swing are 1.5 mA μm^{-1}, 1 mA μm^{-1}, 500 cm^2 V^{-1} s^{-1}, 200 Ω μm and 65 mV dec^{-1}, respectively. These parameters are essential for achieving VLSI of 2D electronics.

3D integration of 2D electronics

3D integration of 2D materials has various applications, as depicted in Fig. 3. These applications can fall into two categories: (1) stacking 2D materials to maximize area utilization and facilitate scaling, and (2) integrating 2D materials or devices on top of silicon-based logic or memory devices. The following sections provide a summary of these topics.

Box 1

Corporate research on 2D transistors

Although it is thought that applying 3D integration to current silicon technology could extend scaling to the end of this decade, the inherent limitations of a bulk semiconductor like silicon will eventually require the integration of sub-3-nm semiconducting channels. Consequently, owing to the theoretical promise of transistor size scaling — that the number of semiconducting channels can be increased by using a 2D material instead of a bulk semiconductor[208] — as well as the substantial research into 2D transition-metal dichalcogenides by academic institutions, semiconductor companies such as Intel, TSMC and IMEC have started to develop transistors based on 2D semiconducting channels, as shown in the table below. Since 2019, corporate research into 2D transition-metal dichalcogenides has accelerated. Examples of the key findings and accomplishments are summarized in the table.

In addition to corporate research on 2D TMDs, various industries are focusing on developing tools and equipment to produce 2D materials. For example, MOCVD manufacturing companies such as Aixtron and Veeco are playing a substantial part in the growth of 2D materials. Moreover, emerging companies like 2D Factory demonstrate potential for scaling 2D material production to the industrial scale. Although graphene is a semi-metal, it shows promise in applications such as electrostatic interference barriers. In this context, Graphenea has emerged as a prominent player in the graphene-manufacturing industry. We believe these industries will make remarkable progress in tool development and the growth of 2D materials, enabling the widespread adoption of 2D electronics.

TSMC	
2019	Made the first top-gated WS_2 *p*-FET on a SiO_x/Si substrate by using channel area-selective chemical vapour deposition (CVD) growth[209].
2020	Obtained a record high ON-state current (V_{ON}) of 390 μA μm^{-1} for CVD-grown monolayer MoS_2 *n*-FET. The contact resistance (R_C) was decreased to ~1.1 kΩ μm for a channel length of 100 nm, and the thickness of the HfO_x gate was scaled down to 10 nm (an equivalent oxide thickness of 2 nm)[210].
2021	Demonstrated an ohmic contact with a near-zero Schottky barrier height and achieved a contact resistance value of 660 Ω μm with Sb contacts. This advance led to the realization of an I_{ON} of 1,000 μA μm^{-1} at a V_{DS} of 2 V. Importantly, these transistors demonstrated robustness under high-temperature treatments (over 300 °C), making them compatible with back-end-of-line (BEOL) processes. The transistors maintain a high I_{ON} of ~375 μA μm^{-1} at a drain voltage of 1 V (ref. 211).
2022	Introduced a technology computer-aided design model that enabled the precise extraction of different device parameters from experimental data of metal–oxide–semiconductor field-effect transistors (MOSFETs) with 2D channel backgated[212]. Drain-current versus back-gate voltage (I_D–V_{BG}) data of transistors with channel lengths ranging from 0.5 μm to 5 μm were used as the experimental data for the model. Reduced the contact resistance of WSe_2 by about 100 times to around 1 kΩ μm by charge transfer from layered oxide materials to WSe_2 (ref. 213). Realized both *n*- and *p*-FETs by using WSe_2. By using Sb or Pt contacts and through the integration of advanced oxide-based encapsulation and doping techniques, a low R_C of 750 Ω μm and 1.8 kΩ μm were achieved for the *p*-FET and *n*-FET, respectively[214].
2023	Demonstrated an impressive R_C value of below 100 Ω μm with reduced contact lengths. Sb-contacted monolayer MoS_2 transistors demonstrated a R_C value of 164 Ω μm for a contact length of 30 nm at a carrier concentration of 1.4×10^{13} cm^{-2} (ref. 215).
Intel	
2021	By using CVD and MBE, MoS_2 *n*-FETs and WSe_2 *p*-FETs were obtained with a contact resistance of around 400 Ω μm for *n*-FETs[216]. Demonstrated the first-time growth of MoS_2, WS_2, WSe_2 and $MoSe_2$ films using metal–organic chemical vapour deposition (MOCVD) on a 300-mm wafer at BEOL temperatures[31]. By using Sb and Ru as contacts, the performance of both *n*-FETs and *p*-FETs were enhanced and a record low R_C of 2.7 kΩ μm was achieved for *p*-FETs[31].
2022	Demonstrated devices with a channel length of 25 nm, nearly negligible drain-induced barrier lowering, and a subthreshold swing of 75 mV dec^{-1}. Additionally, modelling results suggested that a double-gated device could scale down to at least 10 nm with low leakage[208]. Reported the growth of 2D materials on 300-mm substrates at BEOL-compatible temperatures. Additionally, an I_{ON} of 100 μA μm^{-1} was obtained in WSe_2 *p*-FETs (grown at front-end-of-line temperatures)[217].
2023	2D BEOL barriers with the thickness of 10 Å were used as interconnect barriers and reported promising barrier performance on par with their 25 Å tantalum barrier[218].
IMEC	
2020	Double-gated WS_2 transistors featuring a gate length as small as 18 nm were produced within a 300-mm Si complementary metal–oxide–semiconductor (CMOS) fabrication facility[38].
2021	Approximately 90% yield of WS_2 transistors were achieved on 300-mm substrates[219]. The top-gate lengths of WS_2 FETs were scaled down to below 5 nm (ref. 220).
2023	The collective die-to-wafer technique was developed to transfer epitaxial single-layer MX_2 (*M*=Mo, W; *X*=S, Se) films from sapphire to 300-mm target wafers[221].

Stacked 2D FETs

The first demonstration of 3D integrated electronics utilizing stacked 2D materials was reported in 2012 (ref. 129). This work involved the mechanically exfoliated *n*-type MoS_2 on top of a *p*-type $Bi_2Sr_2Co_2O_8$ – a layered transition-metal oxide that can be exfoliated – to create a 3D inverter. The full stack consisted of graphene (for the supply voltage node), $Bi_2Sr_2Co_2O_8$ (*p*-channel), graphene again (for the output node), MoS_2 (*n*-channel) and Ti/Au (the ground) layered on a Si/SiN_x

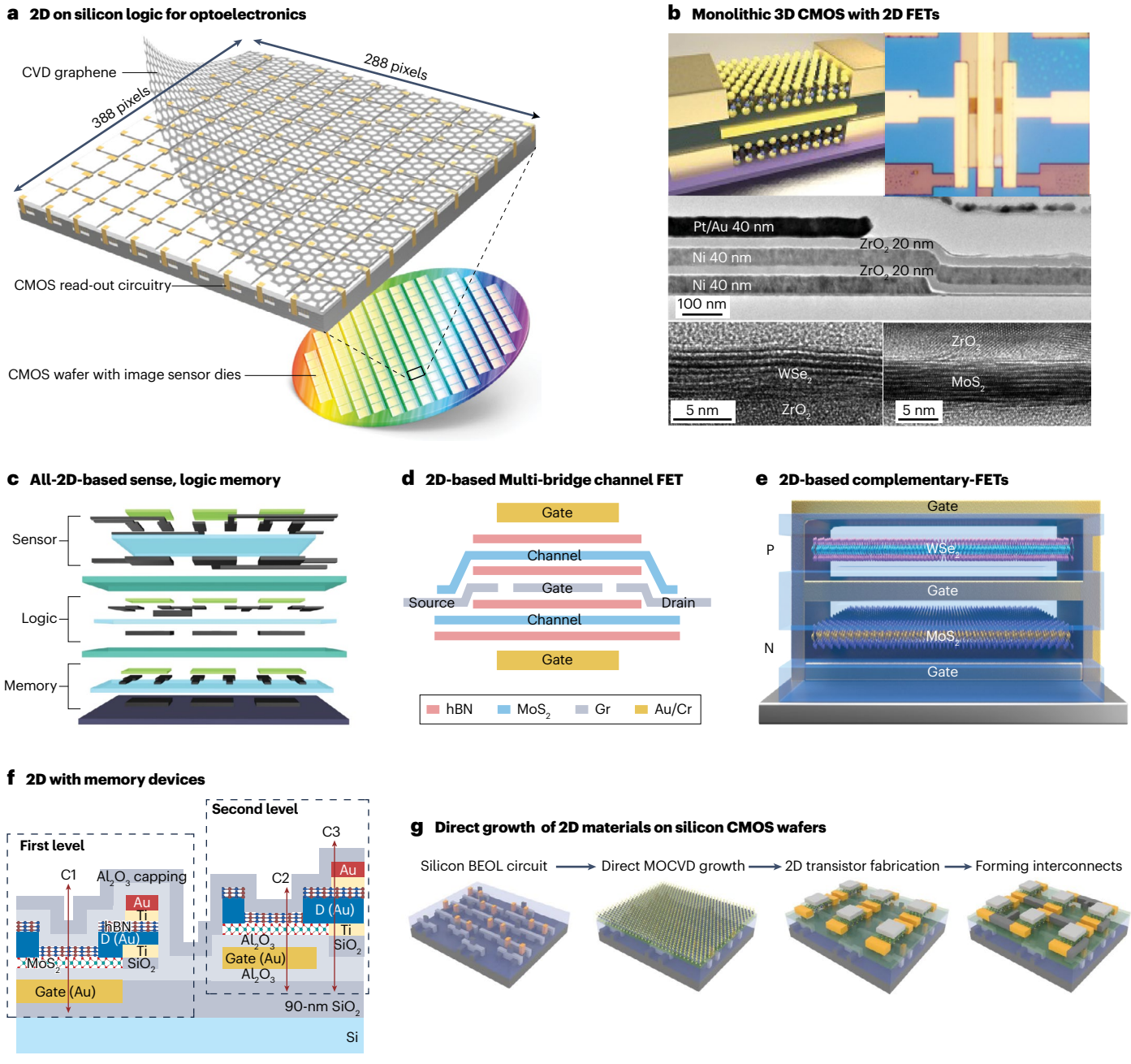

Fig. 3 | Applications of 3D integration of 2D electronics. a, Integration of 2D materials with silicon logic for optoelectronics. **b**, Monolithic 3D complementary metal–oxide–semiconductor (CMOS) with 2D field-effect transistors (FETs). **c**, Incorporation of sensing and memory functionalities with logic, all based on 2D materials. **d**, 2D-based multi-bridge channel FETs. **e**, 2D-based complementary-FETs. **f**, Integration of 2D materials and memory devices. C1 and C2 denote MoS_2-based transistors in first and second levels of 1-transistor/1-resistor memory cells, respectively, and C3 is used to denote the h-BN-based resistive random-access memory (RRAM) in the second level. **g**, Direct growth of 2D materials on silicon CMOS wafers for 2D-silicon heterogeneous 3D integration. h-BN, hexagonal boron nitride; BEOL, back-end-of-line; MOCVD, metal–organic chemical vapour deposition; ZrO_2, zirconium dioxide. Part **a** reproduced from ref. 142, Springer Nature Limited. Part **b** reproduced from refs. 130,131, Wiley. Part **c** reproduced from ref. 133, Wiley. Part **d** adapted with permission from ref. 136, Wiley. Part **e** reproduced from ref. 138, Wiley. Part **f** reproduced from ref. 143, IEEE. Part **g** reproduced from ref. 34, Springer Nature Limited.

substrate[129]. By 2015, advances had been made in the sequential fabrication of MoS_2 FETs, starting with the growth of the first MoS_2 layer on a SiO_2/Si wafer. This process included device fabrication at the first tier, followed by SiO_2 encapsulation, and was repeated for a second-tier device. However, these devices shared a common global back-gate, and the focus was largely on the MOCVD growth of 2D materials on 4-inch SiO_2/Si wafers, rather than on 3D integration[29].

Substantial progress in 3D integration was reported in 2016 (ref. 130) (Fig. 3b), showcasing the use of mechanically exfoliated 3–7-nm-thick MoS_2 and WSe_2 flakes as *n*- and *p*-type channel materials, respectively, with 20-nm-thick ZrO_2 deposited via atomic layer deposition as the gate dielectric. The corresponding NMOS and PMOS devices had gate length/width dimensions of 2 µm/3.3 µm and 2 µm/5.5 µm, respectively. This work resulted in the fabrication of digital (inverter, NAND and NOR) and analog (amplifiers and signal mixers) CMOS circuits, marking a notable achievement in the field. Concurrently, the silicon industry's exploration of nanosheet technology for GAAFETs paralleled proposals for 3D stacking of 2D FETs, aimed at increasing drive currents (535 µA µm^{-1} ON-state currents for a channel length of 370 nm at a V_{DS} of 4.5 V)[131]. With a channel length/width of around 370 nm/2 µm, they were able to increase the drive current by an order of two with the dual-channel FETs.

In 2019, evaporated 8-nm-thick Te thin films were used to fabricate and stack *p*-type FETs to achieve a PMOS logic 3D inverter[132]. In addition, device statistics from around 60 individual *p*-type FETs were also obtained. This period also saw 2D materials being used to integrate sensing or memory functions into 3D ICs. A layer-by-layer stacking approach enabled the demonstration of devices across three tiers (Fig. 3c), utilizing exfoliated few-layer graphene and 45–47-nm-thick hexagonal boron nitride (h-BN) for gate/contact electrodes and dielectrics, respectively, with transferred CVD-grown MoS_2 serving as the semiconducting channel[133]. Consequently, the first, second and third tiers comprised three two-terminal memories, three in-plane inverters and NAND gates, and three individual optical sensing FETs, respectively.

Despite these advances, challenges such as the reliance on mechanical exfoliation and the use of h-BN as the gate dielectric were limiting factors for scaling[134]. Nonetheless, the connection of three vertically stacked FETs demonstrated an increase in current densities (I_{ON} = 54 µA µm^{-1} at V_{DS} = 1 V for a 3-µm channel length), because this design increases the effective width while maintaining the same active device area of a single FET. Further progress in 2021 included the monolithic fabrication of 3D inverters using vertically stacked *n*-type MoS_2 and *p*-type WSe_2 FETs, alongside the use of chemical doping for threshold voltage engineering[135]. Exploration continued with the development of MoS_2-based multi-bridge channel FETs[136] (Fig. 3d) and further demonstrations of 3D-integrated inverter, NAND and NOR circuits using CVD-grown MoS_2 and $MoTe_2$ for *n*-FETs and *p*-FETs, respectively[137]. In these devices, HfO_2 was used as the gate dielectric and the channel length was relatively large at 10–20 µm. The same year, another demonstration involved the fabrication of 22 complementary-FET devices with *p*-type WSe_2 FETs stacked on top of *n*-type MoS_2 FETs[138] (Fig. 3e). CVD was used to grow both 2D materials while HfO_2 deposited by atomic layer deposition was used as the gate dielectric. The channel length and width were both 5 µm. A similar demonstration involved the fabrication of 3D inverters using *p*-type $MoTe_2$ and *n*-type MoS_2 (ref. 139).

The most recent notable advance in 3D-integrated 2D electronics involves the demonstration of (1) wafer-scale and monolithic two-tier 3D integration based on MoS_2 with more than 10,000 FETs in each tier; (2) three-tier 3D integration based on both MoS_2 and WSe_2 with about 500 FETs in each tier; and (3) two-tier 3D integration based on 200 scaled MoS_2 FETs (channel length 45 nm) in each tier[140].

Integrating 2D with logic or memory

2D materials are being explored not only for their potential in scaling FETs but also for incorporation into BEOL transistors and applications. Early developments along this route involved the use of 2D materials for optoelectronic applications. In 2016, researchers successfully transferred CVD-grown MoS_2 onto interlayer-dielectric-encapsulated silicon-based logic or memory tiers on a silicon wafer[141]. The top tier consisted of a 5 × 5 phototransistor array, based on CVD-grown MoS_2, while the bottom tier comprised 6-transistor static random-access memory (6T SRAMs) using poly-silicon nanowire FETs. A transparent conducting oxide served as the top-gate metal, facilitating the light–matter interaction in 2D materials. This work also introduced the idea of using other 2D TMDs with different bandgaps for wavelength-dependent optical sensing.

The substantial potential for monolithic 3D integration of 2D materials with silicon CMOS technology was further demonstrated in 2017 with the development of a 388 × 288-pixel broadband image sensor[142] (Fig. 3a). This sensor was manufactured by transferring CVD-grown graphene onto a pre-fabricated silicon CMOS die, complete with vertical interconnects and read-out circuitry. Lead sulfide colloidal quantum dots were deposited onto the patterned graphene pixels, serving as the light absorption layer. The photodetection mechanism in the device arises from the photogating effect and charge transfer from the quantum dots to the graphene layer, which enables ultrahigh gain and photoresponsivity. The incorporation of graphene remarkably improved the dynamic range, responsivity and broadband detection capabilities (300–2,000 nm), showcasing the benefits of monolithic 3D integration with 2D materials.

Monolithic integration has also been applied to embed memory functionalities into 2D FETs. In 2018, a team demonstrated a two-level stacked 2 × 2 one-transistor, one-resistor (1T1R) array combining local back-gated MoS_2 transistors with h-BN-based resistive random-access memory (RRAM) devices[143] (Fig. 3f). Despite the need for additional planarization steps owing to surface roughness, the fabrication flow emphasized the feasibility of integrating memory devices with 2D FETs in a 3D architecture.

In 2022, another team transferred CVD-grown MoS_2 onto HfO_2-encapsulated *p*-type silicon FETs showcasing 3D inverter and two-input NAND and NOR circuits[144]. The channel lengths and widths of both *n*-FETs and *p*-FETs were 10 µm and 16 µm, respectively. A similar effort led to the monolithic integration of a 3D CMOS inverter, achieved by fabricating top-gated 2D FETs based on CVD-grown MoS_2 on top of silicon finFETs[145]. These advancements highlight ongoing improvements in the transfer process and the development of low-temperature wafer-scale growth techniques for 2D materials. A notable example includes the use of a MOCVD reactor that separates the low-temperature growth region (where the target substrate is placed) from the high-temperature chalcogenide-precursor-decomposition region. This setup enabled the direct growth of MoS_2 on a 200-mm silicon CMOS wafer at temperatures below 300 °C, meeting BEOL temperature requirements and facilitating the heterogeneous integration of a MoS_2–silicon SRAM cell)[34] (Fig. 3g).

Similarly, 2D h-BN (~6 nm) was transferred onto pre-fabricated silicon–CMOS microchip to integrate memristors with silicon CMOS transistors, paving the way for in-memory computing with one-transistor,

one-memristor (1T1M) cells[146]. Beyond electronic applications, 2D materials are also being widely explored for their potential in photonic applications within a 3D-integrated architecture[147]. The most recent notable advance includes the demonstration of an AI-processing hardware using six layers of transistor and memristor arrays based on MoS_2, WSe_2 and h-BN[140]. These authors utilized the capability to peel off a flexible substrate from a rigid carrier substrate after device fabrication and stack it on the target substrate. The work is an important milestone in the path towards enabling next-generation wearable electronics.

Design considerations and challenges

Once reliable 2D-based circuits can be reproducibly manufactured on the large scale, the subsequent objective is to expand this technology into 3D integration, which presents unique challenges that demand dedicated research efforts to address. In this section, we provide a comprehensive evaluation of various design considerations that are critical for the development of 2D-based monolithic 3D ICs. We note that design considerations for electronic devices vary substantially, depending on the desired functionalities the final product is intended to perform. When it comes to heterogeneous monolithic 3D integration — combining different materials, devices and functionalities within a single chip leads to an increase in complexity. Hence, crafting chips for specific tasks requires dedicated designs and specialized process flows. The overarching goals are to improve performance, power efficiency and integration density, to minimize size and costs, to optimize resource allocation and to increase signal speed. We start by examining design considerations related to materials, devices and fabrication techniques, then move to surface planarization, thermal management and reducing electrostatic coupling, and finally conclude with a discussion of the general architectural design principles for 3D ICs.

Materials, devices and fabrication techniques

The selection of devices and functional blocks for a 3D chip is determined by the desired functionalities, which include *n*- and *p*-type 2D FETs, memory devices and sensors for optical, biological and chemical applications, as well as Si-based circuits, among others. Each type of device has its own set of fabrication needs and limitations, which affect the choice of materials and technologies used for creating connections between layers (inter-tier vias), insulating layers between tiers (inter-tier dielectrics), thermal dissipation and electrical interference screening layers. In addition, choosing materials for these different functionalities also requires consideration of their thermal properties, such as the coefficient of thermal expansion and thermal conductivity, as well as their compatibility with the fabrication process.

After the selection of materials for the desired devices, it is crucial to address the fabrication complexities associated with their integration into a 3D chip. For instance, in a Si-based 3D prototype, low-temperature molecular bonding of silicon-on-insulator was used to minimize performance degradation in the bottom tiers[148]. It is essential to evaluate the effect of process variations during the sequential fabrication of top tiers on the performance of bottom-tier devices, particularly in heterogeneous 3D integration. Key issues to consider include the presence of voids at interfaces[149], the quality of inter-tier dielectrics, the occurrence of resistive shorts or opens in circuit connections and vias[150] and electrostatic coupling, as well as impurities and particle contamination introduced during fabrication. Each of these factors can substantially affect the overall performance of the chip across its different tiers.

Surface planarization

2D semiconductors are promising for scaled FETs with sub-1-nm channel thickness. However, the reliability of these scaled FETs faces challenges due to defects caused by surface roughness and irregularities at the interfaces between 2D materials and dielectrics[151]. Moreover, transferring 2D materials onto non-planarized surfaces can introduce strain, negatively affecting device performance[152]. Additionally, the non-uniformity of growth substrates can lead to variability in device performance among different 2D FETs[153], a problem that intensifies when synthesizing 2D materials at low temperatures on various substrates[34]. In 2D FETs utilizing high-κ dielectrics, the importance of smooth surfaces escalates as devices become thinner, to prevent dielectric disorder[154]. Consequently, planarization — a process designed to create uniform, ultra-smooth and defect-free surfaces — is crucial in the semiconductor industry. It enhances lithography and etch yields, mitigates step coverage issues, prevents electromigration, reduces contact resistances and addresses metallization challenges[155].

Currently, chemical mechanical polishing (CMP) is the most widely used planarization technique, achieving ultra-smooth and flat surfaces by combining mechanical forces with chemical reactions[156]. CMP involves pressing the substrate against a rotating polishing pad and applying a polishing slurry, as illustrated in Fig. 4a. This slurry, consisting of chemicals and abrasives, facilitates chemical reactions and, together with the controlled hardness and force applied to the substrate, effectively removes material[157]. The composition of the slurry — abrasives, corrosion inhibitors, complexing agents, pH regulators, and dispersants or surfactants — is tailored to the materials being removed[158]. The interaction of the slurry with different materials at the substrate interface requires careful studies. Determining the optimal material removal rate involves analysing factors such as slurry composition, mechanical force, pad texture and hardness, heat generation and platen rotation velocity[159]. Various models have been developed to analyse wafer–pad contact, lubrication and the chemical reactions between the slurry and metals or dielectrics to prevent defects such as metal dishing, oxide erosion and corrosion[160–162]. Thermal models address issues such as metal film delamination caused by heat during CMP[163–165]. At present, research focuses on reducing defects, developing CMP fill synthesis[166–168], improving post-CMP cleaning methods and creating environmentally friendly slurries[169]. With advances in 2D electronics, testing new materials for semiconducting channels, dielectrics, contacts, vias and interconnects becomes crucial. This emphasizes the need for refined CMP methodologies for 3D ICs based on 2D electronics, requiring thorough analysis of chemical and mechanical interactions at the wafer interfaces[145].

Thermal management

Planar 2D ICs utilize bulk Si, thermal interface materials and heat sink structures for efficient thermal management[170,171]. However, for 3D ICs, the increased device and power density leads to higher heat generation. This issue is compounded by the difficulty of accessing and creating adequate thermal dissipation paths in the upper tiers, exacerbating the impact of heat. Exposure to higher temperatures can cause signal delays and accelerate ageing, thereby reducing the chip's lifetime. Therefore, it is crucial that every design step for a 3D IC incorporates thermal considerations. Effective heat dissipation from thermal hotspots in a 3D IC requires materials with high thermal conductivity and thermal vias or pathways that have a low overall thermal resistance, including at material interfaces. The challenges of thermal management with 2D materials are illustrated in Fig. 4b.

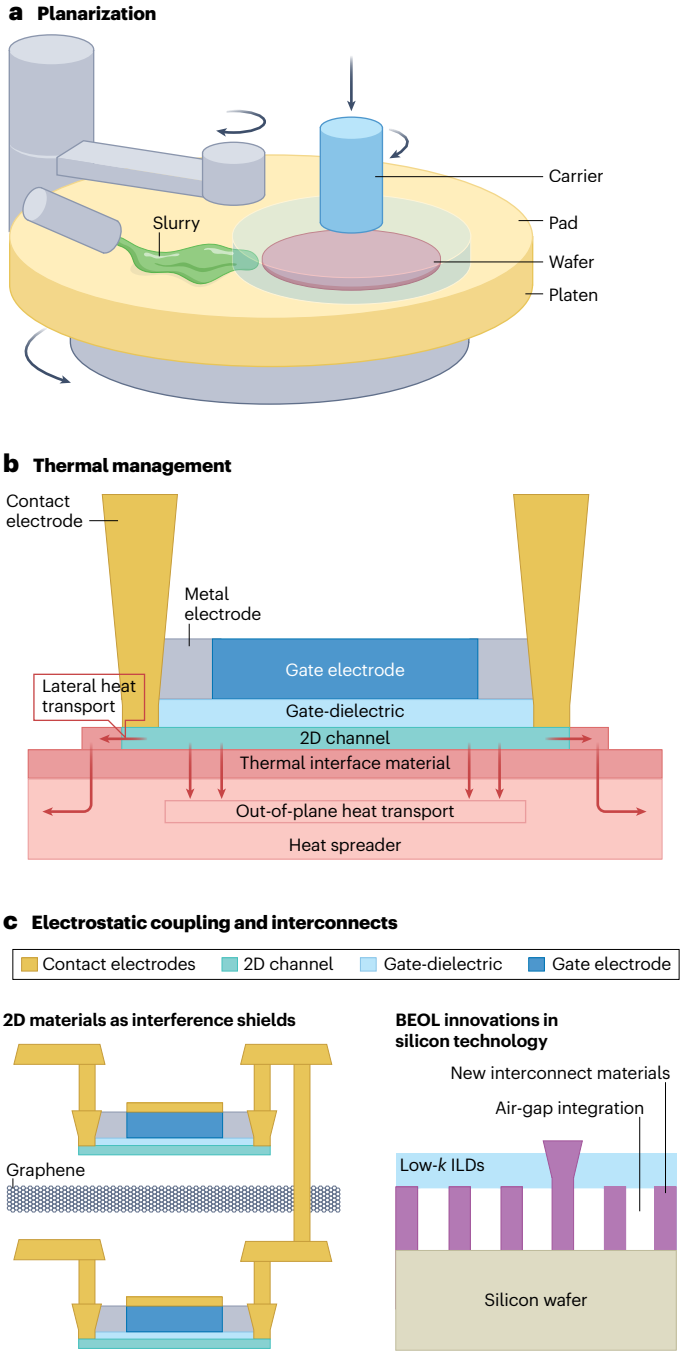

Fig. 4 | Design considerations and challenges for 3D integration with 2D electronics. a, Schematic of a typical chemical mechanical polishing setup consisting of rotating polishing pads, chemical slurry and so on with a wafer carrier. **b**, Thermal management challenges associated with 2D materials. They include high out-of-plane thermal insulation of 2D materials and integration obstacles for heat spreaders. **c**, Electrostatic coupling and interconnects. 2D materials like graphene can potentially be incorporated as barriers to prevent electrostatic interference. Since 2D-based 3D integration can potentially decrease the tier thickness considerably, it is important to keep up with the latest innovations in silicon technology such as back-side power delivery networks, air-gap integration, low-κ interlayer dielectrics (ILDs) and the introduction of new interconnect materials, which may be adopted for 2D electronics. BEOL, back-end-of-line.

Understanding nanoscale thermal transport in 2D FETs often requires advanced theoretical models alongside experimental research[172,173]. Studies have explored localized heat generation in 2D electronics[174], high thermal isolation between van der Waals layers[175], and the effect of thermal expansion coefficient mismatch between 2D materials and substrates[176,177]. However, in some cases, the use of 2D materials demands new characterization techniques[178]. For example, in a recent study, a purely experimental approach to extract the in-plane thermal expansion coefficient of 2D TMD monolayers was presented, thereby addressing the large discrepancies in 2D TMD thermal expansion coefficient values in the literature[179]. In their approach, they utilized Raman spectroscopy to capture the difference in thermal expansion of the 2D material on different substrates caused by the thermal mismatch between the 2D film and the substrate to extract the thermal expansion coefficient. There are also other approaches, using van der Waals materials for both thermal isolation as well as heat-spreading applications. For example, an interesting study reported extremely anisotropic thermal conductors with a room-temperature thermal anisotropy ratio – the ratio of thermal conductivity along the fast axis to that of the slow axis – of 900 for MoS_2 (ref. 180), suggesting that interlayer rotation may be an effective technique to engineer anisotropic thermal properties in 2D materials. Furthermore, graphene and related materials have been shown to be effective heat spreaders, potentially replacing traditional heavier materials such as aluminium and copper[181,182]. These experimental studies are propelling the field towards a more thermal-focused research on 2D VLSI chips. This includes the development of thermally conductive vias, spreaders, heat sinks, microfluidic channels, and other design and packaging solutions for 3D integration of 2D electronics. Various results and techniques mentioned above must be coupled with models and studies of densely integrated chips.

Parasitic capacitance

The impact of parasitic capacitance and electrostatic coupling between conductive elements must be carefully considered in the physical design of 3D ICs, because these can lead to detrimental effects such as signal degradation or delay, noise and crosstalk[183,184]. At the device level, these electricalf interferences can cause unwanted changes in threshold voltage and increased power consumption[149,185]. Therefore, during the layout stage, the routing, placement and spacing between various components should be meticulously analysed to account for capacitive coupling. This analysis necessitates the use of appropriate low-κ dielectric materials, shielding layers and grounding planes[186,187]. However, considerations must also extend to interface properties, thermal conductivity and the coefficient of thermal expansion when selecting materials. Additionally, 2D materials, such as graphene, have been proposed as electrostatic screening layers (Fig. 4c). To enhance the screening efficiency of graphene, even at high-frequency regimes (up to 500 GHz), doping has been proposed, based on evaluations of its electrostatic screening properties[50]. Continuous innovations in silicon technology – including interconnects, power delivery and interlayer dielectrics – remain essential because they are likely to be integrated with 2D electronics in the future.

Architectural design considerations

After determining the desired devices, functionalities, corresponding materials and associated fabrication processes, identifying the optimal integration approach becomes the subsequent crucial step. This requires a comprehensive electrical-design-automation tool flow

to ensure seamless incorporation while upholding the performance standards of the 3D IC[188]. A primary step towards 3D integration is tier partitioning, which involves dividing the 3D IC into distinct tiers based on functionality, fabrication processes, power delivery and thermal management. This division can occur at the transistor level, the block level or the gate level.

At the transistor level, the *n*-type and *p*-type transistors of each standard cell are placed in different tiers without the need for advanced tier-partitioning algorithms. At the block level, tier partitioning divides tiers according to functional blocks, such as logic, memory, power and input–output functionality. Even though block-level tier partitioning simplifies integration complexities, gate-level partitioning offers the most design flexibility. Here, optimization of signal propagation, minimization of interconnect lengths, and improvements in performance and efficiency are achieved by grouping gates and associated interconnects according to the critical paths that minimize connections between critical components for ease of signal propagation, functionality, connectivity, thermal management, clock domains, and so on. There are several methods and algorithms to perform tier-partitioning at the block and gate levels for silicon-based 3D ICs[189–194]. Incorporating thermal analysis and optimization techniques into these tier-partitioning methods is crucial, especially when using 2D materials and thin (less than 1 µm) tiers.

Another critical design step for 3D ICs is 3D placement, where the optimal physical locations of different functional blocks are determined on the basis of signal delays, power distribution, thermal management, and so on. 3D placement approaches (or 3D placers) aim to address performance, voltage-drop and thermal hotspot issues by optimizing routing congestion and critical path timing. They place power-hungry components close to power sources and thermally sensitive components close to heat sinks. There are two types of 3D placer: pseudo-3D placers[195,196], which treat the 3D IC as a planar design using 2D placement algorithms, and true-3D placers[197–199], which consider the 3D vertical stacking nature of IC and inter-tier via connectivity.

Following tier partitioning and 3D placements, the next step is the design of a 3D clock delivery network. This network is crucial for distributing clock signals within a 3D IC, ensuring signal integrity and synchronization of different components to operate at the desired clock frequency. Key considerations include clock distribution, clock tree synthesis, power and ground distribution, crosstalk and noise mitigation, and thermal optimization[200].

There are several approaches and examples of tier partitioning, 3D placers and 3D clock delivery networks, developed for silicon-based 3D ICs and designs based on through-silicon vias, and complemented with thermal analysis and optimization techniques. As 2D electronics matures, modifying current solutions or developing techniques for the physical design of 2D FET-based monolithic 3D ICs will become critical.

3D testing

3D IC testing is the final step in assessing the industrialization potential of 2D-based 3D chips. It is crucial to recognize that various defects and potential faults must be anticipated as testing solutions are developed. Some sources of defects include those arising from fabrication process variations, voids or defects in the interlayer dielectric, and resistive opens or shorts in interconnects or vias[201,202]. Additionally, it is important to consider the effects of heating and ageing on performance degradation in 3D ICs[171]. The effects of various defects will also depend on the design considerations made during the tier partitioning, placing and 3D clock delivery network design steps. Therefore, it is essential to integrate test solutions concurrently with the development of the physical design[188]. Ultimately, expanding current delay fault models[203,204] and associated design-for-test solutions[188,205,206] to accommodate 2D VLSI chips will become critical.

Conclusion

We have delved into diverse topics, including the advance towards very-large-scale integration in 2D electronics, as well as the progress, opportunities and design considerations related to 3D integration of 2D electronics. 3D integration with 2D semiconductors offers remarkable benefits, such as the potential for scaling transistors and increasing device density, and also the development of multifunctional chips through the incorporation of non-computational devices in a 3D architecture. We hope that this Review not only elucidates key considerations in the design of 3D integrated circuits based on 2D materials but also stimulates increased interest in this exciting field.

Published online: 25 April 2024

References

1. Dennard, R. H. et al. Design of ion-implanted MOSFET's with very small physical dimensions. *IEEE J. Solid-State Circ.* **9**, 256–268 (1974).
2. Moore, G. E. Cramming more components onto integrated circuits. *Electronics* **38**, 114–117 (1965).
3. Burg, D. & Ausubel, J. H. Moore's Law revisited through Intel chip density. *PLoS One* **16**, e0256245 (2021).
4. Kelleher, B. Celebrating 75 years of the transistor. A look at the evolution of Moore's Law innovation. In *IEEE Int. Electron Devices Meeting (IEDM)* 1.1.1–1.1.5 (IEEE, 2022).
5. Lau, J. H. State-of-the-art of advanced packaging. In *Chiplet Design and Heterogeneous Integration Packaging* (ed. Lau, J. H.) 1–99 (Springer Nature, 2023).
6. Chen, M. F., Chen, F. C., Chiou, W. C. & Yu, D. C. H. System on integrated chips (SoIC(TM) for 3D heterogeneous integration. In *69th Electronic Components and Technology Conf. (ECTC)* 594–599 (IEEE, 2019).
7. Ingerly, D. B. et al. Foveros: 3D integration and the use of face-to-face chip stacking for logic devices. In *IEEE Int. Electron Devices Meet. (IEDM)* 19.6.1–19.6.4 (IEEE, 2019).
8. Yu, D. TSMC packaging technologies for chiplets and 3D. In *Proc. IEEE Hot Chips* 33 (IEEE, 2021).
9. Lau, J. H. Recent advances and trends in advanced packaging. *IEEE Trans. Compon. Packag. Manuf. Technol.* **12**, 228–252 (2022).
10. Lu, D. & Wong, C. P. (eds) *Materials for Advanced Packaging* Vol. 181 (Springer, 2009).
11. Badaroglu, M. More Moore. In *IEEE Int. Roadmap for Devices and Systems Outbriefs* 1–38 (IEEE, 2021).
12. Vinet, M. et al. Monolithic 3D integration: a powerful alternative to classical 2D scaling. In *SOI-3D-Subthreshold Microelectronics Technology Unified Conf. (S3S)* https://doi.org/10.1109/S3S.2014.7028194 (2014).
13. Shulaker, M. M. et al. Monolithic 3D integration: a path from concept to reality. In *Proc. Design, Automation & Test in Europe Conf. Exhib. (DATE '15)* 1197–1202 (2015).
14. Dhananjay, K., Shukla, P., Pavlidis, V. F., Coskun, A. & Salman, E. Monolithic 3D integrated circuits: recent trends and future prospects. *IEEE Trans. Circ. Syst. II* **68**, 837–843 (2021).
15. Courtland, R. The rise of the monolithic 3-D chip. *IEEE Spect.* **51**, 18–19 (2014).
16. Or-Bach, Z. The monolithic 3D advantage: monolithic 3D is far more than just an alternative to 0.7x scaling. In *IEEE Int. 3D Systems Integration Conf. (3DIC)* https://doi.org/10.1109/3DIC.2013.6702316 (IEEE, 2013).
17. Kunio, T., Oyama, K., Hayashi, Y. & Morimoto, M. Three dimensional ICs, having four stacked active device layers. In *Int. Tech. Digest on Electron Devices Meet.* 837–840 (1989).
18. Gotzlich, J., Kircher, R., Giesen, K. & Poschl, G. Characterization and simulation of SOI-CMOS devices for 3D-integration. In *19th Eur. Solid State Device Research Conf. (ESSDERC '89)* 873–876 (1989).
19. Ferry, D., McGill, T. & Ehrenreich, H. Three dimensional integrated circuits. In *Preliminary Reports, Memoranda and Technical Notes of the Materials Research Council Summer Conf.* 16 (University of Michigan, Department of Materials and Metallurgical Engineering, 1983).
20. Bohr M. T. & Young, I. A. CMOS scaling trends and beyond. *IEEE Micro*. **37**, 20–29 (2017).
21. Ritzenthaler, R. et al. Comparison of electrical performance of co-integrated forksheets and nanosheets transistors for the 2 nm technological node and beyond. In *IEEE Int. Electron Devices Meet. (IEDM)* 26.2.1–26.2.4 (IEEE, 2021).
22. Schuddinck, P. et al. Device-, circuit- & block-level evaluation of CFET in a 4 track library. In *Symp. VLSI Technology* T204–T205 (2019).
23. Jacob, P. et al. Scaling challenges for advanced CMOS devices. *Int. J. High. Speed Electron. Syst.* **26**, 1740001 (2017).
24. Uchida, K. et al. Experimental study on carrier transport mechanism in ultrathin-body SOI NAND p-MOSFETs with SOI thickness less than 5 nm. In *Digest Int. Electron Devices Meet.* 47–50 (IEEE, 2002).

25. Wei, T. et al. Two dimensional semiconducting materials for ultimately scaled transistors. *iScience* **25**, 105160 (2022).
26. Das, S. et al. Transistors based on two-dimensional materials for future integrated circuits. *Nat. Electron.* **4**, 786–799 (2021).
27. Lemme, M. C., Akinwande, D., Huyghebaert, C. & Stampfer, C. 2D materials for future heterogeneous electronics. *Nat. Commun.* **13**, 1392 (2022).
28. Zhu, K. et al. The development of integrated circuits based on two-dimensional materials. *Nat. Electron.* **4**, 775–785 (2021).
29. Kang, K. et al. High-mobility three-atom-thick semiconducting films with wafer-scale homogeneity. *Nature* **520**, 656–660 (2015).
30. Asselberghs, I. et al. Scaled transistors with 2D materials from the 300 mm fab. In *IEEE Silicon Nanoelectronics Worksh. (SNW)* 67–68 (IEEE, 2020).
31. O'Brien, K. P. et al. Advancing 2D monolayer CMOS through contact, channel and interface engineering. In *IEEE Int. Electron Devices Meet. (IEDM)* 11–16 (IEEE, 2021).
32. Liu, L. et al. Uniform nucleation and epitaxy of bilayer molybdenum disulfide on sapphire. *Nature* **605**, 69–75 (2022).
This article describes the uniform nucleation and epitaxy of bilayer MoS_2.
33. Kim, K. S. et al. Non-epitaxial single-crystal 2D material growth by geometric confinement. *Nature* **614**, https://doi.org/10.1038/s41586-022-05524-0 (2023).
34. Zhu, J. et al. Low-thermal-budget synthesis of monolayer molybdenum disulfide for silicon back-end-of-line integration on a 200 mm platform. *Nature Nanotechnol.* **18**, 456–463 (2023).
This article describes low-thermal-budget growth of monolayer MoS_2 on a 200 mm platform.
35. Radisavljevic, A., Radenovic, J., Brivio, V., Giacometti & Kis, A. Single-layer MoS_2 transistors. *Nature Nanotechnol.* **6**, 147–150 (2011).
This article demonstrates the first MoS_2 FET.
36. Desai, S. B. et al. MoS_2 transistors with 1-nanometer gate lengths. *Science* **354**, 99–102 (2016).
37. Wachter, S., Polyushkin, D. K., Bethge, O. & Mueller, T. A microprocessor based on a two-dimensional semiconductor. *Nat. Commun.* **8**, 14948 (2017).
This article reports a microprocessor based on 2D materials.
38. Asselberghs, I. et al. Wafer-scale integration of double gated WS_2-transistors in 300 mm Si CMOS fab. In *IEEE Int. Electron Devices Meet. (IEDM)* 40.2.1–40.2.4 (IEEE, 2020).
39. Shen, P.-C. et al. Ultralow contact resistance between semimetal and monolayer semiconductors. *Nature* **593**, 211–217 (2021).
40. Li, W. et al. Approaching the quantum limit in two-dimensional semiconductor contacts. *Nature* **613**, 274–279 (2023).
The article reports very low contact resistance for Sb-contacted transistors.
41. Jiang, J., Xu, L., Qiu, C. & Peng, L.-M. Ballistic two-dimensional InSe transistors. *Nature* **616**, 470–475 (2023).
This article describes 10-nm ballistic InSe field-effect transistors.
42. Tan, C. et al. 2D fin field-effect transistors integrated with epitaxial high-κ gate oxide. *Nature* **616**, 66–72 (2023).
This article reports 2D fin-shaped field-effect transistors.
43. Chung, Y. Y. et al. First demonstration of GAA monolayer-MoS_2 nanosheet nFET with 410μA μm ID 1V VD at 40 nm gate length. In *IEEE Int. Electron Devices Meet. (IEDM)* 34.5.1–34.5.4 (IEEE, 2022).
This article is the first demonstration of a gate-all-around monolayer-MoS_2 nanosheet *n*-field-effect transistor.
44. Ciarrocchi, F., Tagarelli, A., Avsar & Kis, A. Excitonic devices with van der Waals heterostructures: valleytronics meets twistronics. *Nat. Rev. Mater.* **7**, 449–464 (2022).
45. Sierra, J. F., Fabian, J., Kawakami, R. K., Roche, S. & Valenzuela, S. O. Van der Waals heterostructures for spintronics and opto-spintronics. *Nat. Nanotechnol.* **16**, 856–868 (2021).
46. Schaibley, J. R. et al. Valleytronics in 2D materials. *Nat. Rev. Mater.* **1**, (2016).
47. Miao, F., Liang, S.-J. & Cheng, B. Straintronics with van der Waals materials. *npj Quant. Mater.* **6**, 59 (2021).
48. Daus et al. High-performance flexible nanoscale transistors based on transition metal dichalcogenides. *Nat. Electron.* **4**, 495–501 (2021).
49. Akinwande et al. Graphene and two-dimensional materials for silicon technology. *Nature* **573**, 507–518 (2019).
50. Jiang, J., Parto, K., Cao, W. & Banerjee, K. Ultimate monolithic-3D integration with 2D materials: rationale, prospects, and challenges. *IEEE J. Electron. Devices Soc.* **7**, 878–887 (2019).
51. Lee, Y.-H. et al. Synthesis of large-area MoS_2 atomic layers with chemical vapor deposition. *Adv. Mater.* **24**, 2320–2325 (2012).
52. van der Zande, M. et al. Grains and grain boundaries in highly crystalline monolayer molybdenum disulphide. *Nat. Mater.* **12**, 554–561 (2023).
53. Schram, T. et al. WS_2 transistors on 300 mm wafers with BEOL compatibility. In *2017 47th Eur. Solid-State Device Research Conf. (ESSDERC)* 212–215 (2017).
54. Yang, P. et al. Batch production of 6-inch uniform monolayer molybdenum disulfide catalyzed by sodium in glass. *Nat. Commun.* **9**, 979 (2018).
55. Dumcenco et al. Large-area epitaxial monolayer MoS_2. *ACS Nano* **9**, 4611–4620 (2015).
56. Yu, H. et al. Wafer-scale growth and transfer of highly-oriented monolayer MoS_2 continuous films. *ACS Nano* **11**, 12001–12007 (2017).
57. Li, T. et al. Epitaxial growth of wafer-scale molybdenum disulfide semiconductor single crystals on sapphire. *Nat. Nanotechnol.* **16**, 1201–1207 (2021).
58. Fu, J.-H. et al. Oriented lateral growth of two-dimensional materials on c-plane sapphire. *Nat. Nanotechnol.* **18**, 1289–1294 (2023).
59. Chubarov, M. et al. Wafer-scale epitaxial growth of unidirectional WS_2 monolayers on sapphire. *ACS Nano* **15**, 2532–2541 (2021).
60. Zhu, H. et al. Step engineering for nucleation and domain orientation control in WSe_2 epitaxy on c-plane sapphire. *Nat. Nanotechnol.* **18**, 1295–1302 (2023).
61. Hoang, T. et al. Low-temperature growth of MoS_2 on polymer and thin glass substrates for flexible electronics. *Nat. Nanotechnol.* **18**, 1439–1447 (2023).
62. Chiang, C., Lan, H. Y., Pang, C. S., Appenzeller, J. & Chen, Z. Air-stable P-doping in record high-performance monolayer WSe_2 devices. *IEEE Electron. Device Lett.* **43**, 319–322 (2022).
63. Schranghamer, T. F., Sharma, M., Singh, R. & Das, S. Review and comparison of layer transfer methods for two-dimensional materials for emerging applications. *Chem. Soc. Rev.* **50**, https://doi.org/10.1039/D1CS00706H (2021).
64. Shim, J. et al. Controlled crack propagation for atomic precision handling of wafer-scale two-dimensional materials. *Science* **362**, 665–670 (2018).
65. Kang, K. et al. Layer-by-layer assembly of two-dimensional materials into wafer-scale heterostructures. *Nature* **550**, 229–233 (2017).
66. Phommahaxay, A. et al. The growing application field of laser debonding: from advanced packaging to future nanoelectronics. In *Int. Wafer Level Packaging Conf. (IWLPC)*. https://doi.org/10.23919/IWLPC.2019.8914124 (2019).
67. Li, M. Y. et al. Wafer-scale Bi-assisted semi-auto dry transfer and fabrication of high-performance monolayer CVD WS_2 transistor. In *IEEE Symp. VLSI Technology and Circuits* 290–291 (IEEE, 2022).
68. Liu, F. et al. Disassembling 2D van der Waals crystals into macroscopic monolayers and reassembling into artificial lattices. *Science* **367**, 903–906 (2020).
69. Ghosh, S. et al. Integration of epitaxial monolayer MX_2 channels on 300 mm wafers via collective-die-to-wafer (CoD2W) transfer. In *2023 IEEE Symp. VLSI Technology and Circuits* https://doi.org/10.23919/VLSITechnologyandCir57934.2023.10185215 (IEEE, 2023).
70. Mannix, J. et al. Robotic four-dimensional pixel assembly of van der Waals solids. *Nat. Nanotechnol.* **17**, 361–366 (2022).
71. Schulman, S., Arnold, A. J. & Das, S. Contact engineering for 2D materials and devices. *Chem. Soc. Rev.* **47**, 3037–3058 (2018).
72. Wang, Y. et al. P-type electrical contacts for 2D transition-metal dichalcogenides. *Nature* **610**, 61–66 (2022).
73. Kwon et al. Interaction- and defect-free van der Waals contacts between metals and two- dimensional semiconductors. *Nat. Electron.* **5**, 241–247 (2022).
74. Liu, Y. et al. Approaching the Schottky–Mott limit in van der Waals metal–semiconductor junctions. *Nature* **557**, 696–700 (2018).
75. Liu et al. Graphene-assisted metal transfer printing for wafer-scale integration of metal electrodes and two-dimensional materials. *Nat. Electron.* **5**, 275–280 (2022).
76. Wang, J. et al. Steep slope p-type 2D WSe_2 field-effect transistors with van der waals contact and negative capacitance. In *IEEE Int. Electron Devices Meet. (IEDM)* 22.3.1–22.3.4 (IEEE, 2018).
77. Yang, X. et al. Highly reproducible van der Waals integration of two-dimensional electronics on the wafer scale. *Nat. Nanotechnol.* **18**, 471–478 (2023).
78. Jung, Y. et al. Transferred via contacts as a platform for ideal two-dimensional transistors. *Nat. Electron.* **2**, 187–194 (2019).
79. Huang, J.-K. et al. High-κ perovskite membranes as insulators for two-dimensional transistors. *Nature* **605**, 262–267 (2022).
80. Lu, Z. et al. Wafer-scale high-κ dielectrics for two-dimensional circuits via van der Waals integration. *Nat. Commun.* **14**, 2340 (2023).
81. Zhang et al. Single-crystalline van der Waals layered dielectric with high dielectric constant. *Nat. Mater.* **22**, 832–837 (2023).
82. Dolui, I., Rungger, C., Das Pemmaraju & Sanvito, S. Possible doping strategies for MoS_2 monolayers: an ab initio study. *Phys. Rev. B* **88,** 075420 (2013).
83. Chowdhury, S., Venkateswaran, P. & Somvanshi, D. A systematic study on the electronic structure of 3D, 4D, and 5D transition metal-doped WSe_2 monolayer. *Superlattices Microstruct.* **148**, 106746 (2020).
84. Suh et al. Doping against the native propensity of MoS_2: degenerate hole doping by cation substitution. *Nano Lett.* **14**, 6976–6982 (2014).
85. Kozhakhmetov, A. et al. Controllable p-type doping of 2D WSe_2 via vanadium substitution. *Adv. Funct. Mater.* **31**, 2105252 (2021).
86. Zhang, K. et al. Tuning the electronic and photonic properties of monolayer MoS_2 via in situ rhenium substitutional doping. *Adv. Funct. Mater.* **28**, 1706950 (2018).
87. Torsi, R. et al. Dilute rhenium doping and its impact on defects in MoS_2. *ACS Nano* **17**, 15629–15640 (2020).
88. Zhang, L. et al. Tuning electrical conductance in bilayer MoS_2 through defect-mediated interlayer chemical bonding. *ACS Nano* **14**, 10265–10275 (2020).
89. Zou, J. et al. Doping concentration modulation in vanadium-doped monolayer molybdenum disulfide for synaptic transistors. *ACS Nano* **15**, 7340–7347 (2021).
90. Jiang, J. et al. Probing giant Zeeman shift in vanadium-doped WSe2 via resonant magnetotunneling transport. *Phys. Rev. B* **103**, 014441 (2021).
91. Li, S. et al. Tunable doping of rhenium and vanadium into transition metal dichalcogenides for two-dimensional electronics. *Adv. Sci.* **8**, e2004438 (2021).
92. Zhao, Y. et al. Doping, contact and interface engineering of two-dimensional layered transition metal dichalcogenides transistors. *Adv. Funct. Mater.* **27**, 1603484 (2017).

93. Stesmans, B., Schoenaers & Afanas, V. V. Variations of paramagnetic defects and dopants in geo-MoS_2 from diverse localities probed by ESR. *J. Chem. Phys.* **152**, 234702 (2020).
94. Tan, M. Z., Freysoldt, C. & Hennig, R. G. First-principles investigation of charged dopants and dopant-vacancy defect complexes in monolayer MoS2. *Phys. Rev. Mater.* **4**, 114002 (2020).
95. Zhang, F. et al. Carbon doping of WS_2 monolayers: bandgap reduction and p-type doping transport. *Sci. Adv.* **5**, eaav5003 (2019).
96. Tang et al. Direct n- to p-type channel conversion in monolayer/few-layer WS_2 field- effect transistors by atomic nitrogen treatment. *ACS Nano* **12**, 2506–2513 (2018).
97. Huang et al. Selective engineering of chalcogen defects in MoS_2 by low-energy helium plasma. *ACS Appl. Mater. Interf.* **11**, 24404–24411 (2019).
98. Luo, P. et al. Doping engineering and functionalization of two-dimensional metal chalcogenides. *Nanoscale Horiz.* **4**, 26–51 (2019).
99. Zhang, X., Shao, Z., Zhang, X., He, Y. & Jie, J. Surface charge transfer doping of low-dimensional nanostructures toward high-performance nanodevices. *Adv. Mater.* **28**, 10409–10442 (2016).
100. Arnold, A. J., Schulman, D. S. & Das, S. Thickness trends of electron and hole conduction and contact carrier injection in surface charge transfer doped 2D field effect transistors. *ACS Nano* **14**, 13557–13568 (2020).
101. Yamamoto, S., Nakaharai, K., Ueno & Tsukagoshi, K. Self-limiting oxides on WSe_2 as controlled surface acceptors and low-resistance hole contacts. *Nano Lett.* **16**, 2720–2727 (2016).
102. McClellan, J., Yalon, E., Smithe, K. K. H., Suryavanshi, S. V. & Pop, E. High current density in monolayer MoS_2 doped by AlO_x. *ACS Nano* **15**, 1587–1596 (2021).
103. Rai et al. Air stable doping and intrinsic mobility enhancement in monolayer molybdenum disulfide by amorphous titanium suboxide encapsulation. *Nano Lett.* **15**, 4329–4336 (2015).
104. Cai, L. et al. Rapid flame synthesis of atomically thin MoO_3 down to monolayer thickness for effective hole doping of WSe_2. *Nano Lett.* **17**, 3854–3861 (2017).
105. Chen, K. et al. Air stable n-doping of WSe_2 by silicon nitride thin films with tunable fixed charge density. *APL Mater.* **2**, 092504 (2014).
106. Choi & Lee, J. C. Scaling equivalent oxide thickness with flat band voltage (VFB) modulation using in situ Ti and Hf interposed in a metal/high-κ gate stack. *J. Appl. Phys.* **108**, 064107 (2010).
107. Lee, H. et al. Dipole doping effect in MoS_2 field effect transistors based on phase transition of ferroelectric polymer dopant. *Original Res.* **10**, https://doi.org/10.3389/fmats.2023.1139954 (2023).
108. Lee et al. Remote modulation doping in van der Waals heterostructure transistors. *Nat. Electron.* **4**, 664–670 (2021).
109. Wu, X. et al. Dual gate synthetic MoS_2 MOSFETs with 4.56μF/cm^2 channel capacitance, 320μS/μm Gm and 420 μA/μm Id at 1V Vd/100 nm Lg. In *IEEE Int. Electron Devices Meet. (IEDM)* 7.4.1–7.4.4 (IEEE, 2021).
110. Waltl, M. et al. Perspective of 2D integrated electronic circuits: scientific pipe dream or disruptive technology? *Adv. Mater.* **34**, 2201082 (2022).
111. Mandyam, S. V., Kim, H. M. & Drndic, M. Large area few-layer TMD film growths and their applications. *J. Phys. Mater.* **3**, 024008 (2010).
112. Kalanyan et al. Rapid wafer-scale growth of polycrystalline 2H-MoS_2 by pulsed metal–organic chemical vapor deposition. *Chem. Mater,* **29**, 6279–6288 (2017).
113. Amani, M. et al. Growth-substrate induced performance degradation in chemically synthesized monolayer MoS_2 field effect transistors. *Appl. Phys. Lett.* **104**, https://doi.org/10.1063/1.4873680 (2014).
114. Li, W. et al. Uniform and ultrathin high-κ gate dielectrics for two-dimensional electronic devices. *Nat. Electron.* **2**, 563–571 (2019).
115. Lau, S. et al. Dielectrics for two-dimensional transition-metal dichalcogenide applications. *ACS Nano* **17**, 9870–9905 (2023).
116. Illarionov, Y. Y. et al. Insulators for 2D nanoelectronics: the gap to bridge. *Nat. Commun.* **11**, 3385 (2020).
117. Illarionov, Y. Y. et al. Ultrathin calcium fluoride insulators for two-dimensional field-effect transistors. *Nat. Electron.* **2**, 230–235 (2019).
118. O'Brien, K. P. et al. Process integration and future outlook of 2D transistors. *Nat. Commun.* **14**, 6400 (2023).
This article provides an outlook on the future of 2D transistors.
119. Sebastian, R., Pendurthi, T. H., Choudhury, J. M., Redwing & Das, S. Benchmarking monolayer MoS_2 and WS_2 field-effect transistors. *Nat. Commun.* **12**, 693 (2021).
120. Weber, O. et al. High immunity to threshold voltage variability in undoped ultra-thin FDSOI MOSFETs and its physical understanding. In *IEEE Int. Electron Devices Meet.* https://doi.org/10.1109/IEDM.2008.4796663 (IEEE, 2008).
121. Bhoir, M. S. et al. Variability sources in nanoscale bulk finFETs and TiTaN — a promising low variability WFM for 7/5 nm CMOS nodes. In *IEEE Int. Electron Devices Meet. (IEDM)* https://doi.org/10.1109/IEDM19573.2019.8993660 (IEEE, 2019).
122. Jiang, J., Xu, L., Qiu, C. & Peng, L.-M. Ballistic two-dimensional InSe transistors. *Nature* **616**, 470–475 (2023).
123. Wang, Y. & Chhowalla, M. Making clean electrical contacts on 2D transition metal dichalcogenides. *Nat. Rev. Phys.* **4**, 101–112 (2022).
124. Wang, Y. et al. Van der Waals contacts between three-dimensional metals and two-dimensional semiconductors. *Nature* **568**, 70–74 (2019).
125. Pang, C.-S. et al. Atomically controlled tunable doping in high-performance WSe_2 devices. *Adv. Electron. Mater.* **6**, 1901304 (2020).
126. Ji, H. G. et al. Chemically tuned p- and n-type WSe_2 monolayers with high carrier mobility for advanced electronics. *Adv. Mater.* **31**, 1903613 (2019).
127. Wu, R. et al. Bilayer tungsten diselenide transistors with on-state currents exceeding 1.5 milliamperes per micrometre. *Nat. Electron.* **5**, 497–504 (2022).
128. Liu, Y. et al. Promises and prospects of two-dimensional transistors. *Nature* **591**, 43–53 (2021).
129. Yu, W. J. et al. Vertically stacked multi-heterostructures of layered materials for logic transistors and complementary inverters. *Nat. Mater.* **12**, 246–252 (2023).
This article is the first demonstration of stacked 2D materials for electronics.
130. Sachid, B. et al. Monolithic 3D CMOS using layered semiconductors. *Adv. Mater.* **28**, 2547–2554 (2016).
131. Zhou, R. & Appenzeller, J. Three-dimensional integration of multi-channel MoS_2 devices for high drive current FETs. In *76th Device Research Conf. (DRC)* https://doi.org/10.1109/DRC.2018.8442137 (IEEE, 2018).
132. Zhao et al. Evaporated tellurium thin films for p-type field-effect transistors and circuits. *Nat. Nanotechnol.* **15**, 53–58 (2020).
133. Tang, J. et al. Vertical integration of 2D building blocks for all-2D electronics. *Adv. Electron. Mater.* **6**, 2000550 (2020).
134. Knobloch, T. et al. The performance limits of hexagonal boron nitride as an insulator for scaled CMOS devices based on two-dimensional materials. *Nat. Electron.* **4**, 98–108 (2021).
135. Xiong, X. et al. Demonstration of vertically-stacked CVD monolayer channels: MoS_2 nanosheets GAA-FET with ion > 700 μA/μm and MoS_2/WSe_2 CFET. In *IEEE Int. Electron Devices Meet. (IEDM)* 7.5.1–7.5.4 (IEEE, 2021).
136. Huang, X. et al. Ultrathin multibridge channel transistor enabled by van der Waals assembly. *Adv. Mater.* **33**, 2102201 (2021).
137. Xia, Y. et al. Wafer-scale demonstration of MBC-FET and C-FET arrays based on two- dimensional semiconductors. *Small* **18**, 2107650 (2022).
138. Liu, M. et al. Large-scale ultrathin channel nanosheet-stacked CFET based on CVD 1L MoS2/WSe_2. *Adv. Electron. Mater.* **9**, 2200722 (2023).
139. Jia, X. et al. High-performance CMOS inverter array with monolithic 3D architecture based on CVD-grown n-MoS_2 and p-$MoTe_2$. *Small* **19**, 2207927 (2023).
140. Kang, J. H. et al. Monolithic 3D integration of 2D materials-based electronics towards ultimate edge computing solutions. *Nat. Mater.* **22**, 1470–1477 (2023).
This article discusses monolithic 3D integration of 2D materials-based electronics towards ultimate edge computing solutions.
141. Yang, C.-C. et al. Enabling monolithic 3D image sensor using large-area monolayer transition metal dichalcogenide and logic/memory hybrid 3D+IC. In *IEEE Symp. VLSI Technology.* https://doi.org/10.1109/VLSIT.2016.7573448 (IEEE, 2016).
142. Goossens, S. et al. Broadband image sensor array based on graphene–CMOS integration. *Nat. Photon.* **11**, 366–371 (2017).
143. Wang, C.-H. et al. 3D monolithic stacked 1T1R cells using monolayer MoS_2 FET and hBN RRAM fabricated at low (150° C) temperature. In *IEEE Int. Electron Devices Meet. (IEDM)* 22.5.1–22.5.4 (IEEE, 2018).
144. Tong, L. et al. Heterogeneous complementary field-effect transistors based on silicon and molybdenum disulfide. *Nat. Electron.* **6**, 37–44 (2023).
145. Guan, S.-X. et al. Monolithic 3D integration of back-end compatible 2D material FET on Si finFET. *npj 2D Mater. Appl.* **7**, 9 (2023).
146. Zhu, K. et al. Hybrid 2D–CMOS microchips for memristive applications. *Nature* **618**, 57–62 (2023).
147. Meng, Y. et al. Photonic van der Waals integration from 2D materials to 3D nanomembranes. *Nat. Rev. Mater.* **8**, 498–517 (2023).
148. Ko, C.-T. & Chen, K.-N. Low temperature bonding technology for 3D integration. *Microelectron. Reliab.* **52**, 302–311 (2012).
149. Koneru, A., Kannan, S. & Chakrabarty, K. Impact of electrostatic coupling and wafer-bonding defects on delay testing of monolithic 3D integrated circuits. *ACM J. Emerg. Technol. Comput. Syst.* **13**, (2017).
150. Chaudhuri, S. et al. Built-in self-test for inter-layer vias in monolithic 3D ICs. In *2019 IEEE Eur. Test Symp. (ETS)* https://doi.org/10.1109/ETS.2019.8791515 (IEEE, 2019).
151. Smets, Q. et al. Sources of variability in scaled MoS_2 FETs. In *IEEE Int. Electron Devices Meet. (IEDM)* 3.1.1–3.1.4 (IEEE, 2020).
152. Shin, G. et al. Indirect bandgap puddles in monolayer MoS_2 by substrate-induced local strain. *Adv. Mater.* **28**, 9378–9384 (2016).
153. Smithe, K. K. H., Suryavanshi, S. V., Muñoz Rojo, M., Tedjarati, A. D. & Pop, E. Low variability in synthetic monolayer MoS_2 devices. *ACS Nano* **11**, 8456–8463 (2017).
154. Raja et al. Dielectric disorder in two-dimensional materials. *Nat. Nanotechnol.* **14**, 832–837 (2019).
155. Zantye, B., Kumar, A. & Sikder, A. Chemical mechanical planarization for microelectronics applications. *Mater. Sci. Eng. R* **45**, 89–220 (2004).
156. Banerjee, G. & Rhoades, R. L. Chemical mechanical planarization historical review and future direction. *ECS Trans.* **13**, https://doi.org/10.1149/1.2912973 (2008).
157. Das, S. Kibria, G., Doloi, B. & Bhattacharyya, *B. Advances in Abrasive Based Machining and Finishing Processes* (Springer, 2020).
158. Zhong, Z.-W. Recent developments and applications of chemical mechanical polishing. *Int. J. Adv. Manuf. Technol.* **109**, 1419–1430 (2020).
159. Seo, J. A review on chemical and mechanical phenomena at the wafer interface during chemical mechanical planarization. *J. Mater. Res.* **36**, 235–257 (2021).
160. Zhao, G. et al. Review on modeling and application of chemical mechanical polishing. *Nanotechnol. Rev.* **9**, 182–189 (2020).

161. Zhao, D. & Lu, X. Chemical mechanical polishing: theory and experiment. *Friction* **1**, 306–326 (2013).
162. Krishnan, M., Nalaskowski, J. W. & Cook, L. M. Chemical mechanical planarization: slurry chemistry, materials, and mechanisms. *Chem. Rev.* **110**, 178–204 (2010).
163. Hocheng, Y. L., Huang & Chen, L. J. Kinematic analysis and measurement of temperature rise on a pad in chemical mechanical planarization. *J. Electrochem. Soc.* **146**, 4236 (1999).
164. White, J., Melvin & Boning, D. Characterization and modeling of dynamic thermal behavior in CMP. *J. Electrochem. Soc.* **150**, G271 (2003).
165. Oh, S. & Seok, J. Modeling of chemical–mechanical polishing considering thermal coupling effects. *Microelectronic Eng.* **85**, 2191–2201 (2008).
166. Khursheed, K., Khare & Haque, F. Z. Automation of optimal metal density filling for deep sub-micron technology designs. *Mater. Today Proc.* **74**, 207–212 (2023).
167. Jiang, B. et al. FIT: fill insertion considering timing. In *Proc. 56th Ann. Design Automation Conf.* https://doi.org/10.1145/3316781.3317826 (ACM, 2019).
168. Kahng, B. & Samadi, K. CMP fill synthesis: a survey of recent studies. *IEEE Trans. Comput. Des. Integr. Circuits Syst.* **27**, 3–19 (2008).
169. Liu, L. et al. A review: green chemical mechanical polishing for metals and brittle wafers. *J. Phys. D* **54**, 373001 (2021).
170. Sarvar, D. C., Whalley & Conway, P. P. Thermal interface materials — a review of the state of the art. *2006 1st Electron. System Integration Technol. Conf.* **2**, 1292–1302 (2006).
171. Lin, S.-C. & Banerjee, K. Thermal challenges of 3D ICs. In *Wafer Level 3-D ICs Process Technology* (eds Tan, C. S., Gutmann, R. J. & Reif, L. R.) 1–26 (Springer, 2008).
172. Cahill, G. et al. Nanoscale thermal transport. II. 2003–2012. *Appl. Phys. Rev.* **1**, 011305 (2014).
173. Liu, X. & Zhang, Y.-W. Thermal properties of transition-metal dichalcogenide. *Chin. Phys. B* **27**, 034402 (2018).
174. Yalon, E. et al. Energy dissipation in monolayer MoS_2 electronics. *Nano Lett.* **17**, 3429–3433 (2017).
175. Vaziri, S. et al. Ultrahigh thermal isolation across heterogeneously layered two-dimensional materials. *Sci. Adv.* **5**, eaax1325 (2019).
176. Wang et al. Difference analysis model for the mismatch effect and substrate-induced lattice deformation in atomically thin materials. *Phys. Rev. B* **98**, 245403 (2018).
177. Zhang & Zhang, Y.-W. Thermal properties of two-dimensional materials. *Chin. Phys. B* **26**, 034401 (2017).
178. Wang, Y., Xu, N., Li, D. & Zhu, J. Thermal properties of two dimensional layered materials. *Adv. Funct. Mater.* **27**, 1604134 (2017).
179. Zhong, Y. et al. A unified approach and descriptor for the thermal expansion of two-dimensional transition metal dichalcogenide monolayers. *Sci. Adv.* **8,** eabo3783 (2022).
180. Kim, S. E. et al. Extremely anisotropic van der Waals thermal conductors. *Nature* **597**, 660–665 (2021).
181. Fu, Y. et al. Graphene related materials for thermal management. *2D Mater.* **7**, 012001 (2020).
182. Ghosh, S. et al. Extremely high thermal conductivity of graphene: prospects for thermal management applications in nanoelectronic circuits. *Appl. Phys. Lett.* **92**, 121911 (2008).
183. Lee, D., Das, S., Doppa, J. R., Pande, P. P. & Chakrabarty, K. Impa ct of electrostatic coupling on monolithic 3D-enabled network on chip. *ACM Trans. Des. Autom. Electron. Syst.* **24**, (2019).
184. Xu, C. & Banerjee, K. Physical modeling of the capacitance and capacitive coupling noise of through-oxide vias in FDSOI-based ultra-high density 3-D ICs. *IEEE Trans. Electron. Dev.* **60**, 123–131 (2012).
185. Batude, P. et al. Advances in 3D CMOS sequential integration. In *IEEE Int. Electron Devices Meet. (IEDM)* https://doi.org/10.1109/IEDM.2009.5424352 (IEEE, 2009).
186. Pragathi, D. et al. An extensive survey on reduction of noise coupling in TSV based 3D IC integration. *Mater. Today Proc.* **45**, 1471–1480 (2021).
187. Kim, S. K., Liu, C. C., Xue, L. & Tiwari, S. Crosstalk reduction in mixed-signal 3-D integrated circuits with interdevice layer ground planes. *IEEE Trans. Electron. Dev.* **52**, 1459–1467 (2005).
188. Zhu, L. et al. Design automation and test solutions for monolithic 3D ICs. *ACM J. Emerg. Technol. Comput. Syst.* **18**, (2021).
189. Samal, S. K., Nayak, D., Ichihashi, M. Banna, S. & Lim, S. K. Tier partitioning strategy to mitigate BEOL degradation and cost issues in monolithic 3D ICs. In *IEEE/ACM Int. Conf. Computer-Aided Design (ICCAD)* https://doi.org/10.1145/2966986.2967080 (ACM, 2016).
190. Guler & Jha, N. K. Hybrid monolithic 3-D IC floorplanner. *IEEE Trans. Very Large Scale Integr. Syst.* **26**, 1868–1880 (2018).
191. Berhault, G., Brocard, M., Thuries, S., Galea, F. & Zaourar, L. 3DIP: an iterative partitioning tool for monolithic 3D IC. In *IEEE Int. 3D Systems Integration Conf. (3DIC)* https://doi.org/10.1109/3DIC.2016.7970013 (IEEE, 2016).
192. Bamberg, L., García-Ortiz, A., Zhu, L., Pentapati, S. & Lim, S. K. Macro-3D: a physical design methodology for face-to-face-stacked heterogeneous 3D ICs. In *Design, Automation & Test in Europe Conf. Exhib. (DATE)* 37–42 (IEEE, 2020).
193. Lu, Y.-C., Pentapati, S. S. K., Zhu, L., Samadi, K. & Lim, S. K. TP-GNN: a graph neural network framework for tier partitioning in monolithic 3D ICs. In *57th ACM/IEEE Design Automation Conf. (DAC)* https://doi.org/10.1109/DAC18072.2020.9218582 (IEEE, 2020).
194. Chang, K. et al. Cascade2D: a design-aware partitioning approach to monolithic 3D IC with 2D commercial tools. In *IEEE/ACM Int. Conf. Computer-Aided Design (ICCAD)* https://doi.org/10.1145/2966986.2967013 (ACM, 2020).
195. Panth, S., Samadi, K., Du, Y. & Lim, S. K. Shrunk-2-D: a physical design methodology to build commercial-quality monolithic 3-D ICs. *IEEE Trans. Comput. Des. Integr. Circuits Syst.* **36**, 1716–1724 (2017).
196. Ku, W., Chang, K. & Lim, S. K. Compact-2D: a physical design methodology to build two- tier gate-level 3-D ICs. *IEEE Trans. Comput. Des. Integr. Circuits Syst.* **39**, 1151–1164 (2019).
197. Cong, J. & Luo, G. A multilevel analytical placement for 3D ICs. In *Asia and South Pacific Design Automation Conf.* 361–366 (IEEE, 2009).
198. Hsu, M.-K., Chang, Y.-W. & Balabanov, V. TSV-aware analytical placement for 3D IC designs. In *Proc. 48th Design Automation Conf.* 664–669 (2011).
199. Lu, J., Zhuang, H., Kang, I., Chen, P. & Cheng, C.-K. ePlace-3D: electrostatics based placement for 3D-ICs. In *Proc. 2016 Int. Symp. Physical Design (ISPD '16)* 11–18 (ACM, 2016).
200. Minz, J., Zhao, X. & Lim, S. K. Buffered clock tree synthesis for 3D ICs under thermal variations. In *Asia and South Pacific Design Automation Conf.* 504–509 (IEEE, 2008).
201. Campregher, N., Cheung, P. Y., Constantinides, G. A. & Vasilko, M. Analysis of yield loss due to random photolithographic defects in the interconnect structure of FPGAs. In *Proc. 2005 ACM/SIGDA 13th Int. Symp. Field-Programmable Gate Arrays* 138–148 (2005).
202. Patterson, D., Wildman, H., Gal, D. & Wu, K. Detection of resistive shorts and opens using voltage contrast inspection. In *17th Ann. SEMI/IEEE ASMC 2006 Conf.* 327–333 (IEEE, 2006).
203. Bernardi, P., Sonza Reorda, M., Bosio, A., Girard, P. & Pravossoudovitch, S. On the modeling of gate delay faults by means of transition delay faults. In *2011 IEEE Int. Symp. on Defect and Fault Tolerance in VLSI and Nanotechnology Systems* 226–232 (IEEE, 2011).
204. Pomeranz & Reddy, S. M. Transition path delay faults: a new path delay fault model for small and large delay defects. *IEEE Trans. VLSI Syst.* **16**, 98–107 (2007).
205. Erb, D., Scheibler, K., Sauer, M., Reddy, S. M. & Becker, B. Multi-cycle circuit parameter independent ATPG for interconnect open defects. In *IEEE 33rd VLSI Test Symp. (VTS)* https://doi.org/10.1109/VTS.2015.7116296 (IEEE, 2015).
206. Koneru, A., Kannan, S. & Chakrabarty, K. A design-for-test solution based on dedicated test layers and test scheduling for monolithic 3-D integrated circuits. *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **38**, 1942–1955 (2018).
207. Jayachandran, D. et al. Three-dimensional integration of two-dimensional field-effect transistors. *Nature* **625**, 276–281 (2024).
This article demonstrates large-scale 3D integration of 2D FETs.
208. Dorow, J. et al. Gate length scaling beyond Si: mono-layer 2D channel FETs robust to short channel effects. In *IEEE Int. Electron Devices Meet. (IEDM)* 7.5.1–7.5.4 (IEEE, 2022).
209. Cheng, C. C. et al. First demonstration of 40-nm channel length top-gate WS_2 pFET using channel area-selective CVD growth directly on SiO_x/Si substrate. In *2019 Symp. VLSI Technology* T244–T245 (2019).
210. Chou, A.-S. et al. High on-current 2D nFET of 390 μA/μm at VDS=1V using monolayer CVD MoS_2 without intentional doping. In *IEEE Symp. VLSI Technology* https://doi.org/10.1109/VLSITechnology18217.2020.9265040 (IEEE, 2020).
211. Chou, A.-S. et al. Antimony semimetal contact with enhanced thermal stability for high performance 2D electronics. In *IEEE Int. Electron Devices Meet. (IEDM)* 7.2.1–7.2.4 (IEEE, 2021).
212. Sathaiya, M. et al. Comprehensive physics based TCAD model for 2D MX2 channel transistors. In *IEEE Int. Electron Devices Meet. (IEDM)* 28.4.1–28.4.4 (IEEE, 2022).
213. Su, S. K. et al. Perspective on low-dimensional channel materials for extremely scaled CMOS. In *IEEE Symp. VLSI Technology and Circuits* 403–404 (IEEE, 2022).
214. Chou, A. S. et al. High-performance monolayer WSe_2 p/n FETs via antimony-platinum modulated contact technology towards 2D CMOS electronics. In *Int. Electron Devices Meet. (IEDM)* https://doi.org/10.1109/IEDM45625.2022.10019491 (IEEE, 2022).
215. Wu, W. C. et al. Scaled contact length with low contact resistance in monolayer 2D channel transistors. In *IEEE Symp. VLSI Technology and Circuits* https://doi.org/10.23919/VLSITechnologyandCir57934.2023.10185408 (IEEE, 2023).
216. Dorow, J. et al. Advancing monolayer 2D NMOS and PMOS transistor integration from growth to van der Waals interface engineering for ultimate CMOS scaling. In *Symp. VLSI Technology* 1–2 (IEEE, 2021).
217. Maxey, K. et al. 300 mm MOCVD 2D CMOS materials for more (than) Moore scaling. In *IEEE Symp. VLSI Technology and Circuits* 419–420 (IEEE, 2022).
218. Naylor, H. et al. 2D Materials in the BEOL. In *IEEE Symp. VLSI Technology and Circuits* https://doi.org/10.23919/VLSITechnologyandCir57934.2023.10185307 (IEEE, 2023).
219. Schram, T. et al. High yield and process uniformity for 300 mm integrated WS_2 FETs. In *Symp. VLSI Technology* 1–2 (2021).
220. Smets, Q. et al. Scaling of double-gated WS_2 FETs to sub-5nm physical gate length fabricated in a 300 mm FAB. In *IEEE Int. Electron Devices Meet. (IEDM)* 34.2.1–34.2.4 (IEEE, 2021).
221. Brems, S. et al. Overview of scalable transfer approaches to enable epitaxial 2D material integration. In *Int. VLSI Symp. Technology, Systems and Applications (VLSI-TSA/VLSI-DAT)* 1–2 (2023).

Author contributions

S.D. conceptualized this work and secured resources. D.J. and N.U.S. researched data for the article, structured and wrote the manuscript. D.J., N.U.S. and S.D. reviewed the manuscript before submission.

Competing interests

The authors declare no competing interests.

Additional information

Peer review information *Nature Reviews Electrical Engineering* thanks the anonymous reviewer(s) for their contribution to the peer review of this work.

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